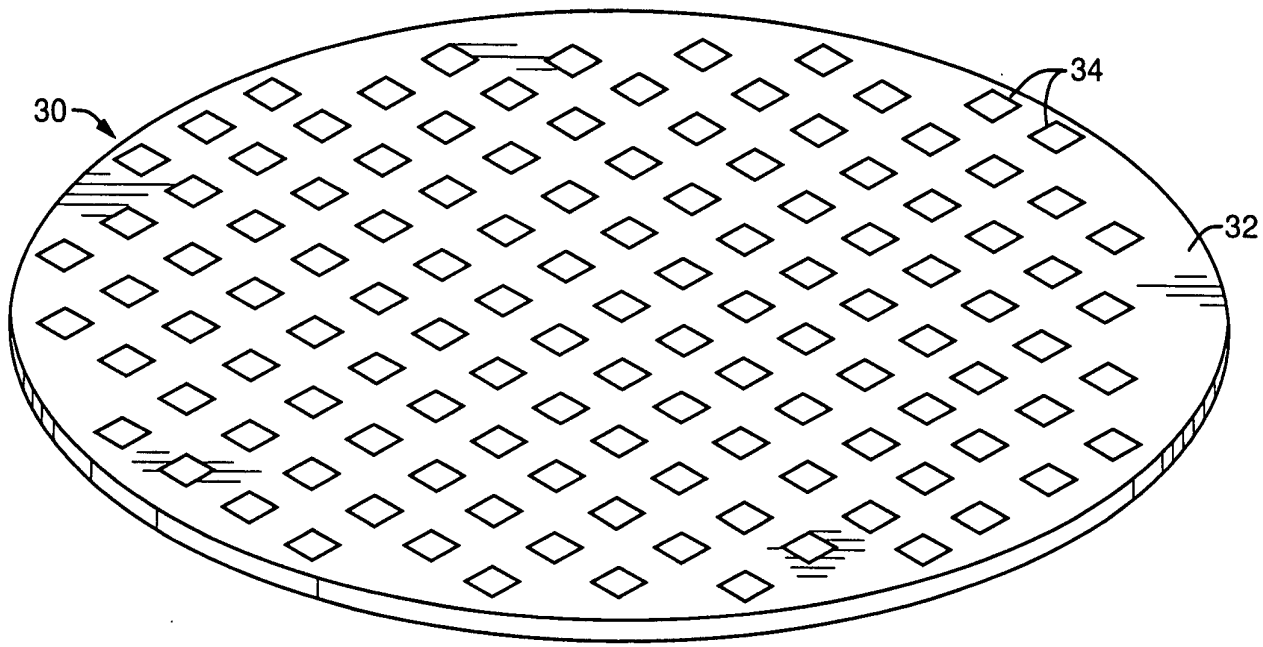


FIG. 1

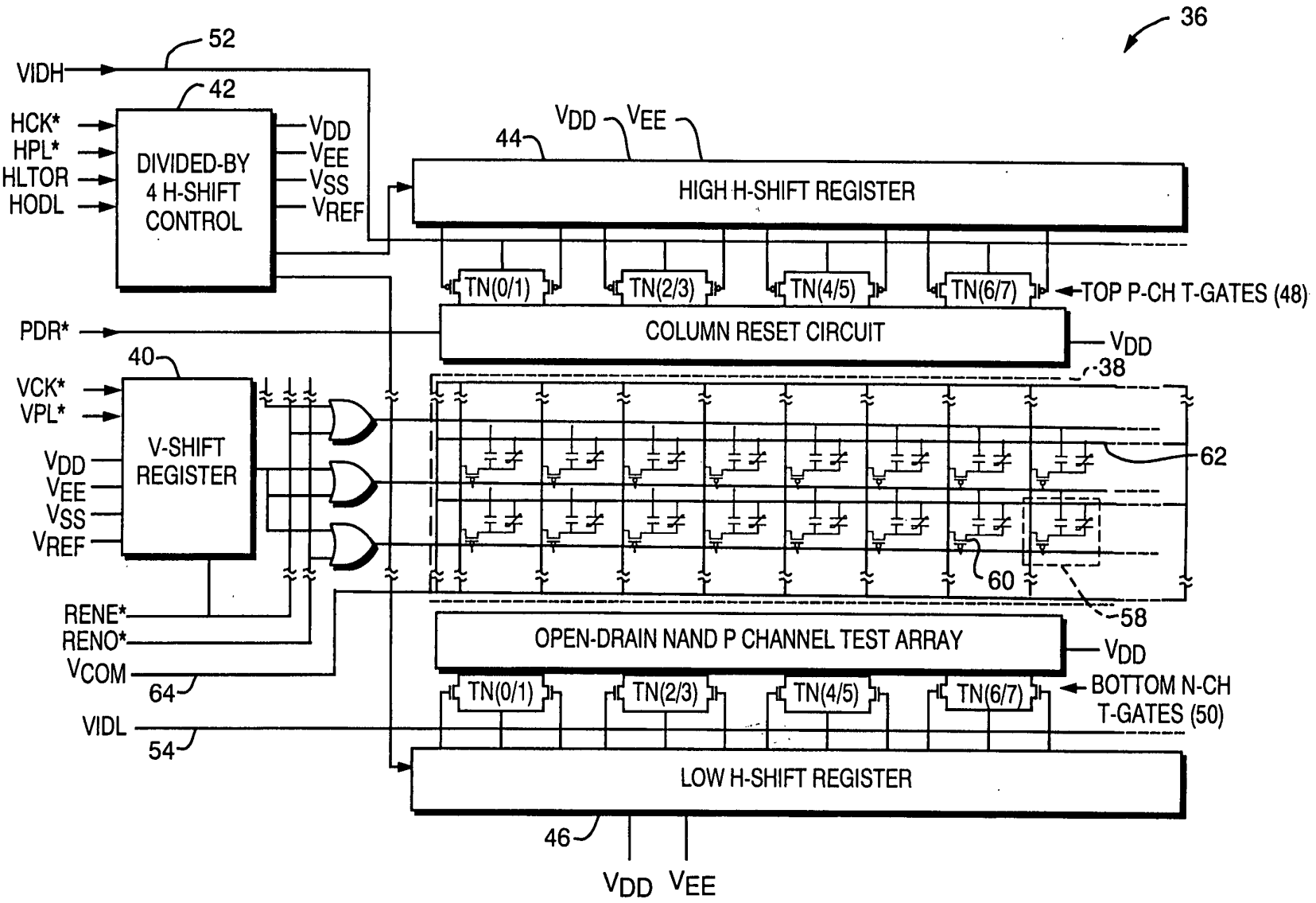


FIG. 2A

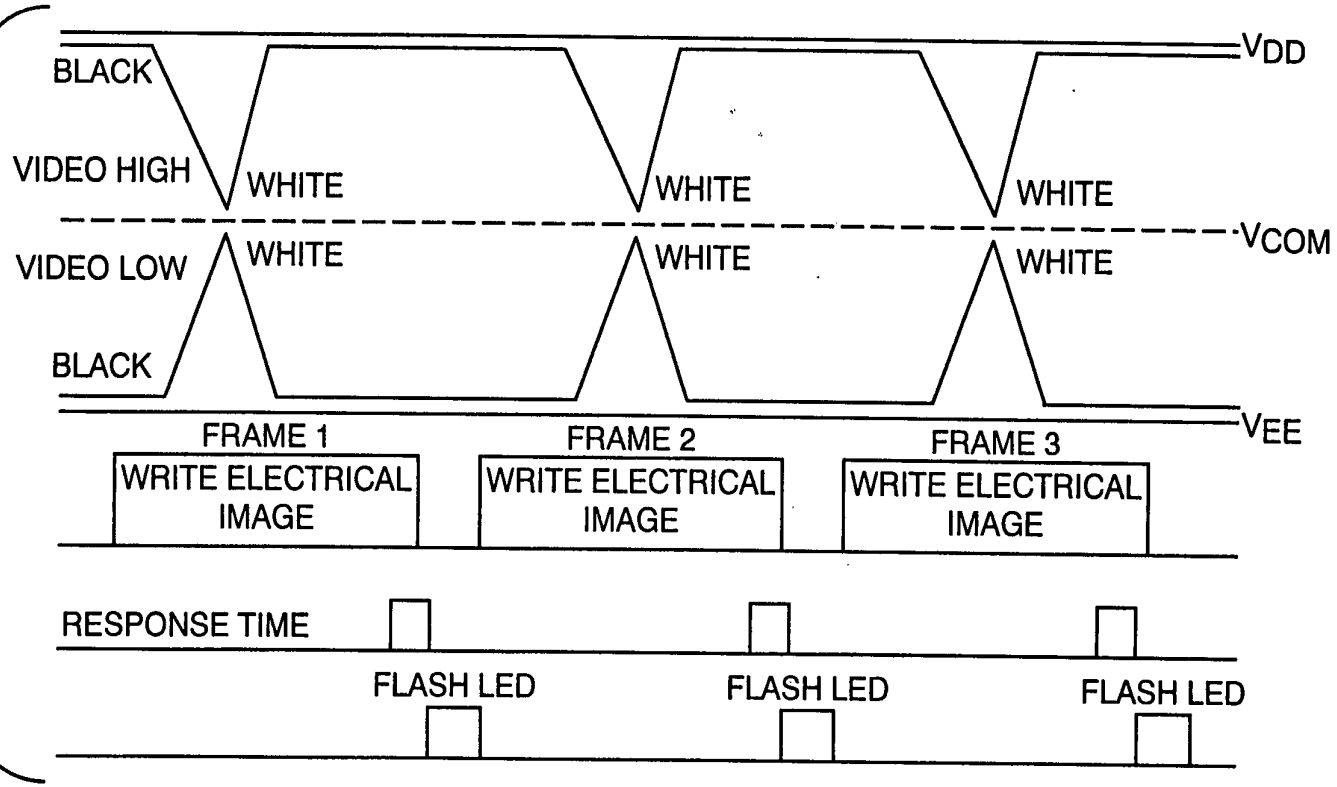


FIG. 2B

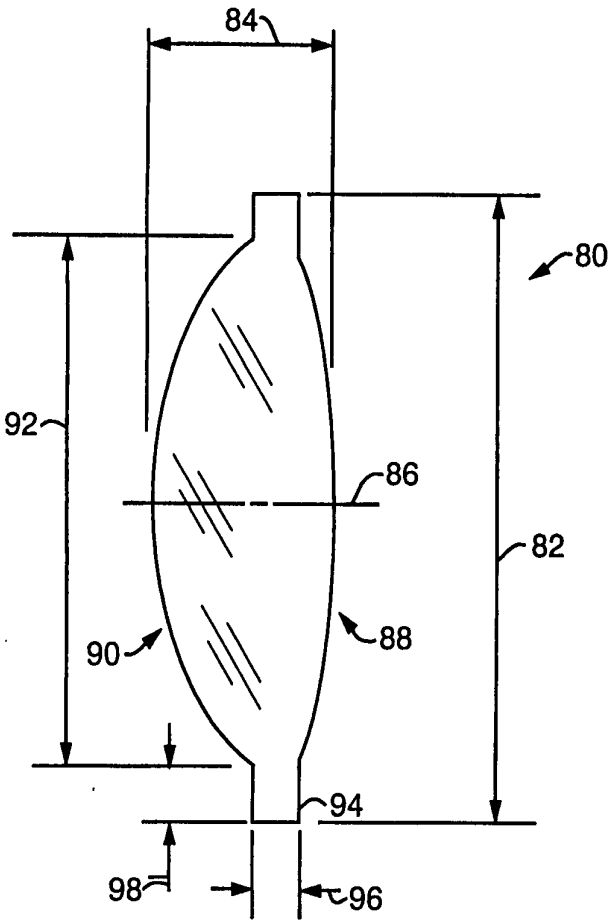


FIG. 3A

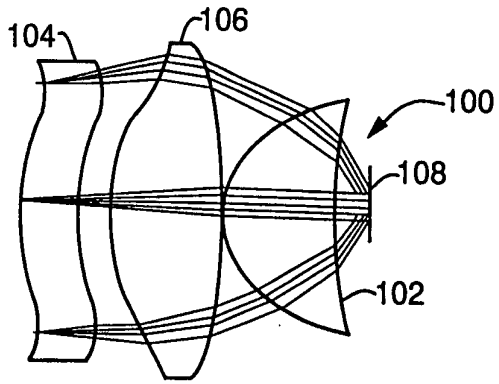


FIG. 3B

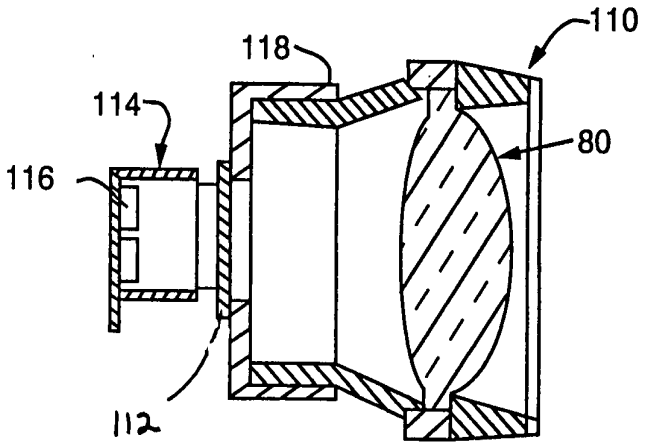


FIG. 3C

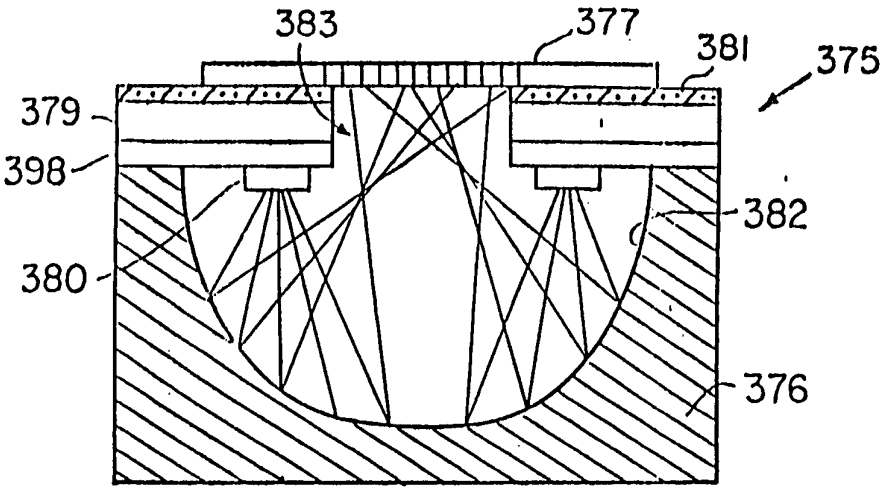


FIG. 3E

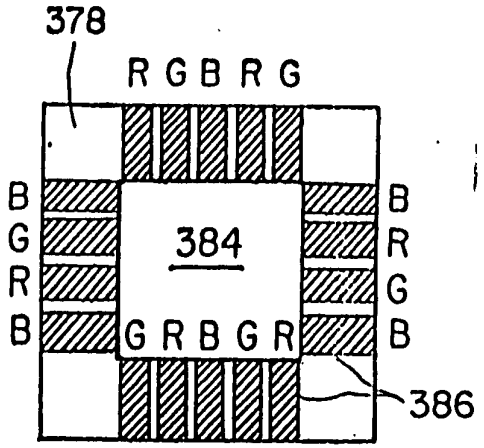


FIG. 3F

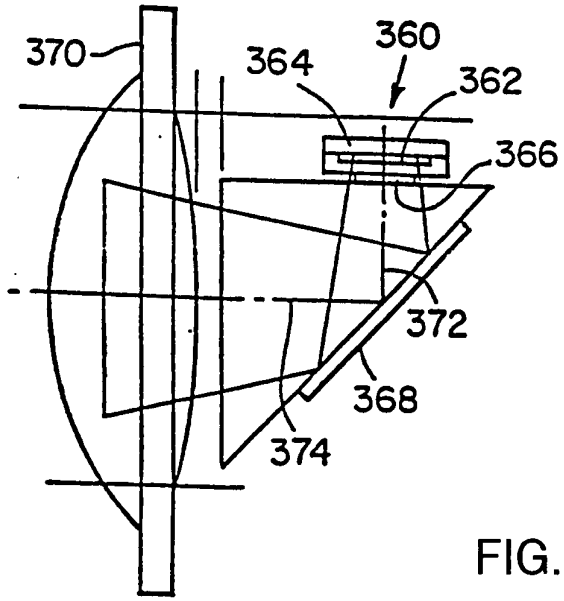


FIG. 3D

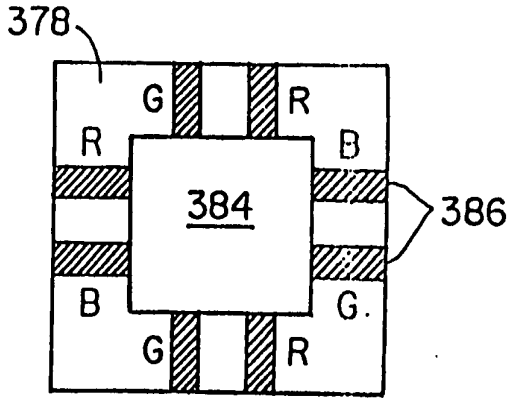


FIG. 3G

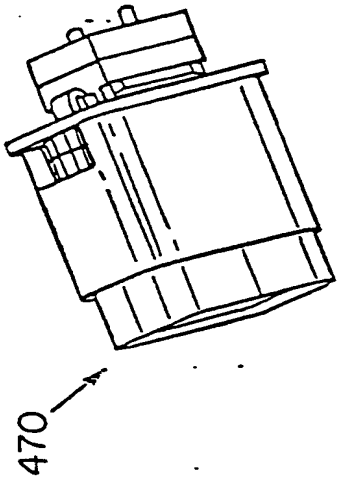


FIG. 3H

FIG. 3I

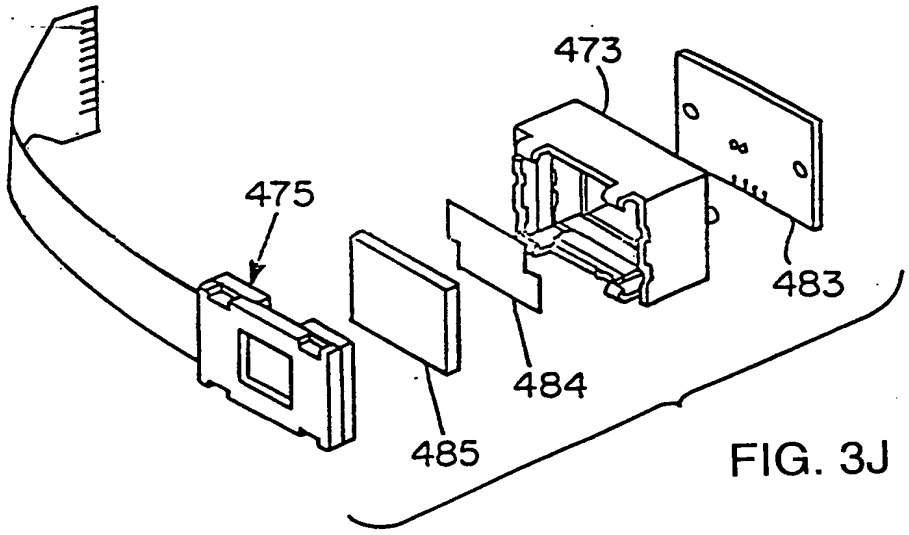


FIG. 3J

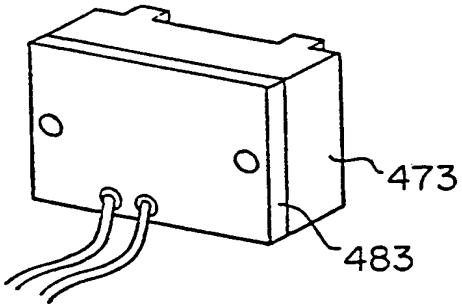


FIG. 3K

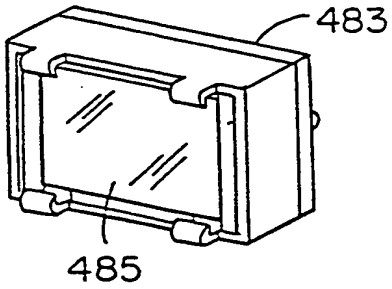


FIG. 3L

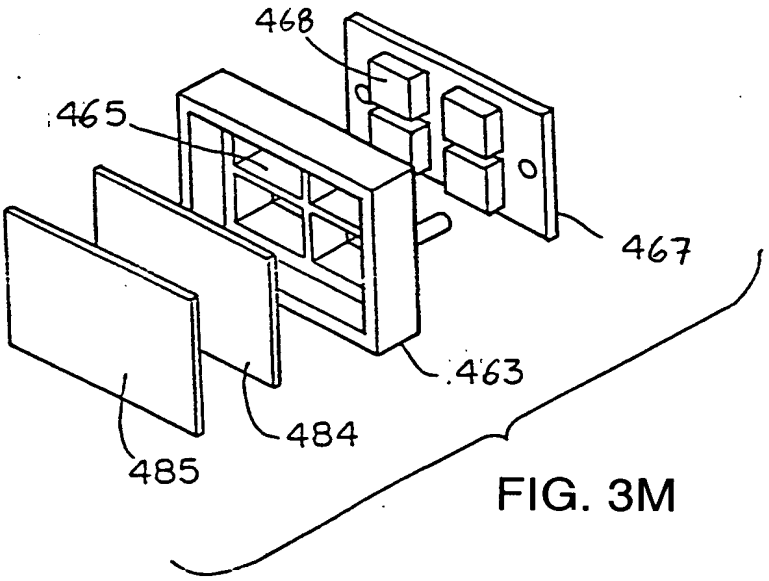


FIG. 3M

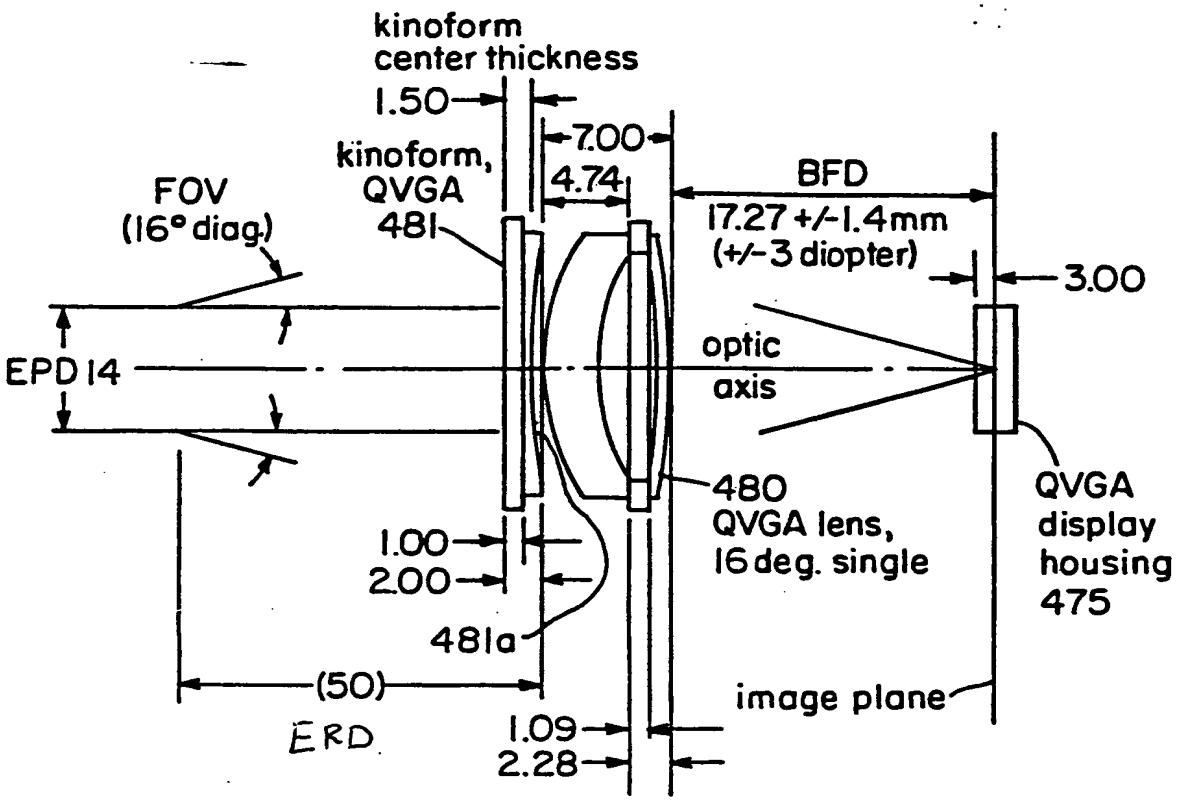

kinoform
center thickness
1.50
7.00
4.74
kinoform,
QVGA
481
FOV
(16° diag.)
BFD
17.27 +/-1.4mm
(+/-3 diopter)
3.00
EPD 14
optic
axis
480
QVGA lens,
16 deg. single
QVGA
display
housing
475
1.00
2.00
481a
(50)
ERD
image plane
1.09
2.28

FIG. 3N

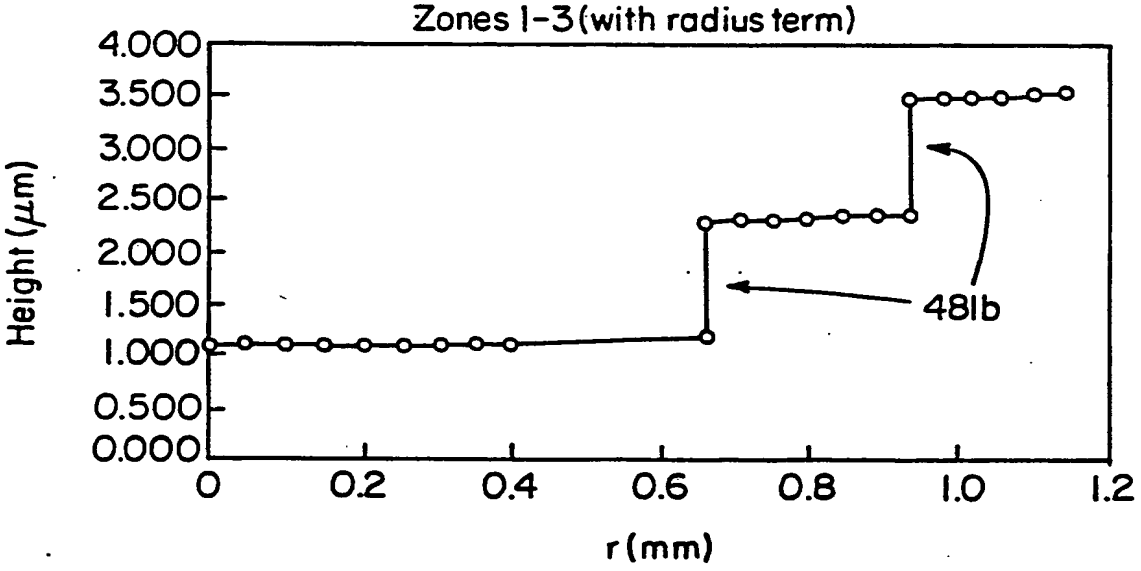

Zones 1-3 (with radius term)
Height (μm)
4.000
3.500
3.000
2.500
2.000
1.500
1.000
0.500
0.000
0
0.2
0.4
0.6
0.8
1.0
1.2
r (mm)
481b

FIG. 3O

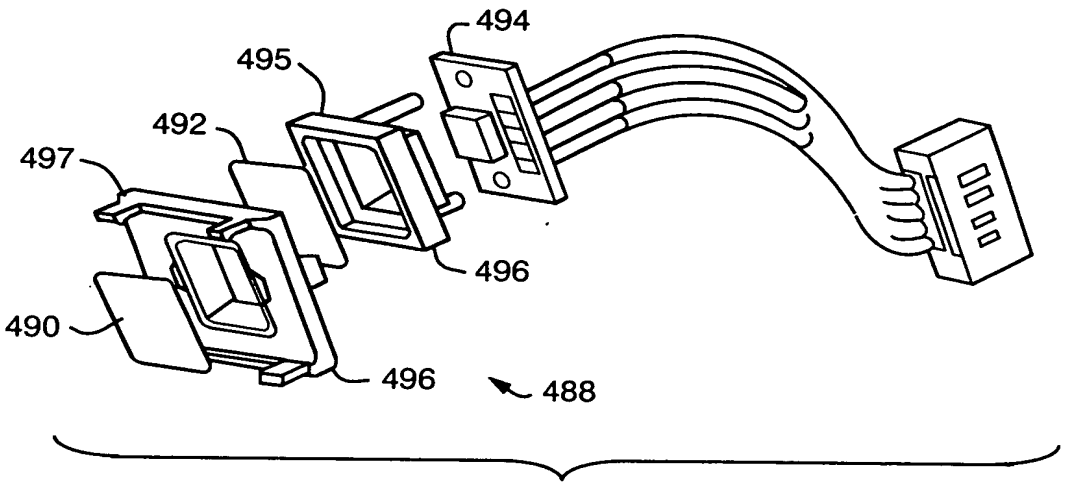


FIG. 3P

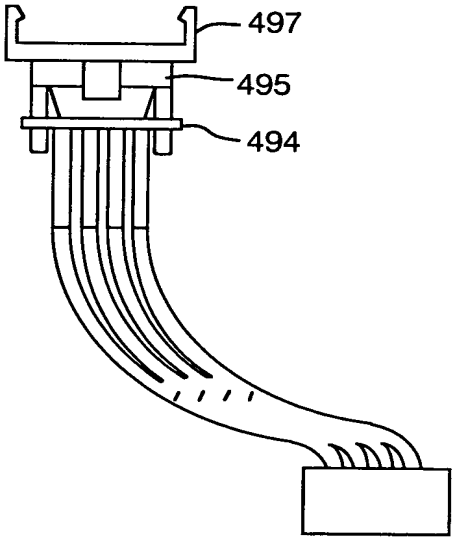


FIG. 3Q

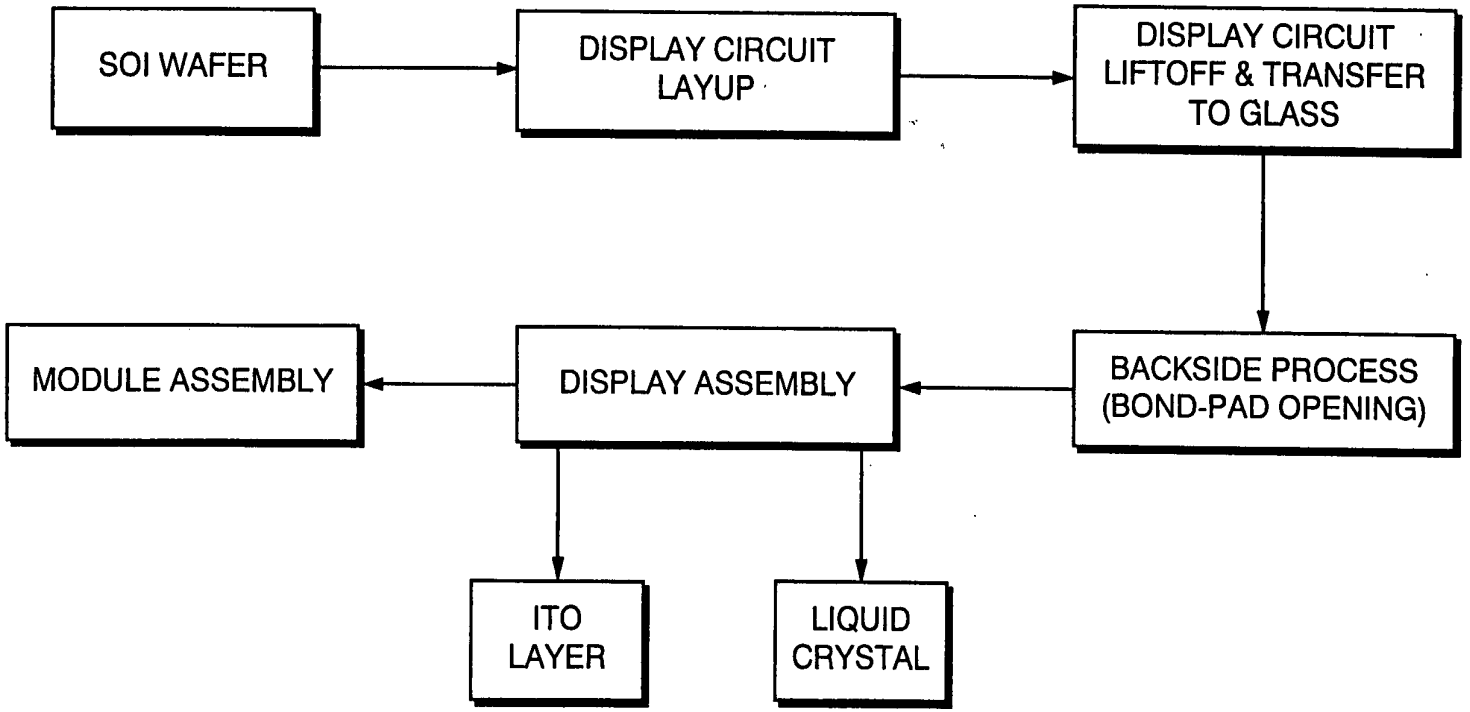


FIG. 4

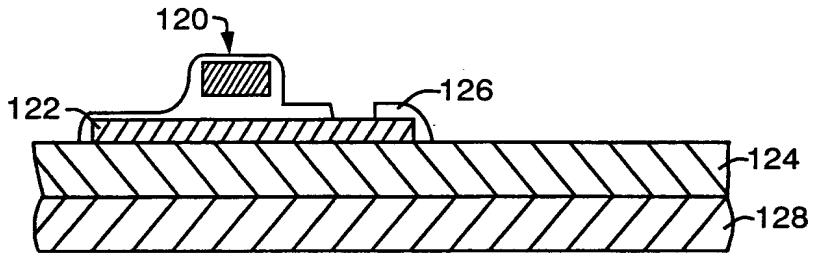


FIG. 5A

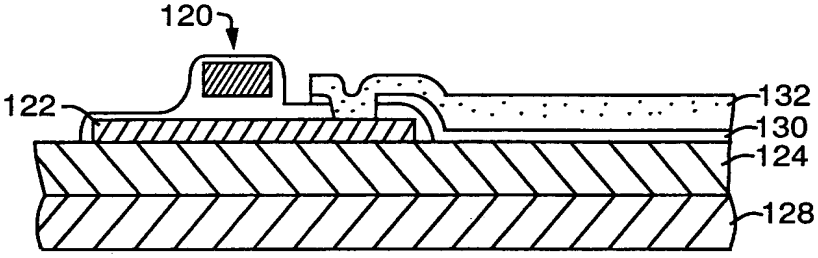


FIG. 5B

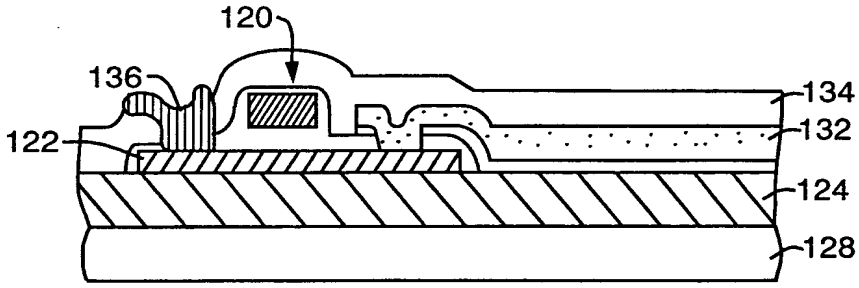


FIG. 5C

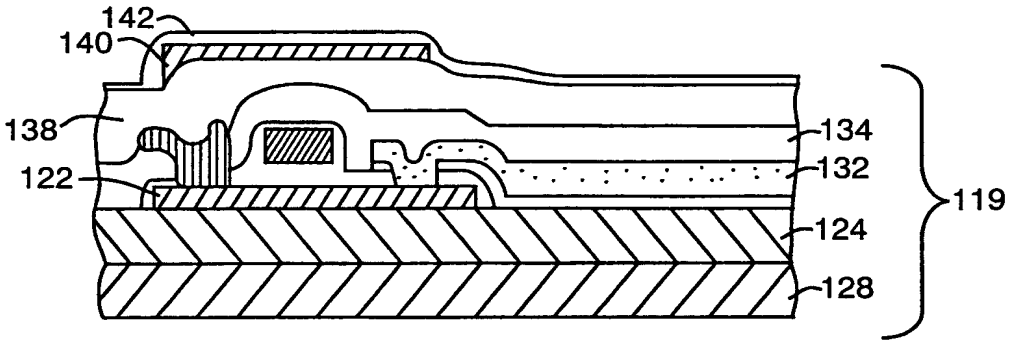


FIG. 5D

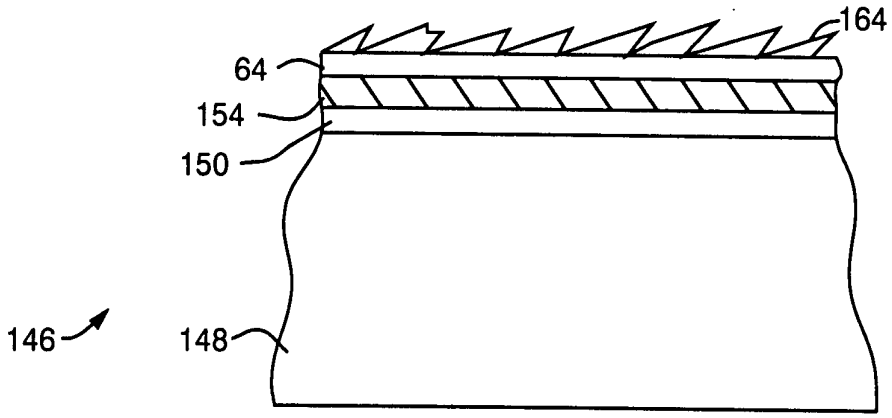


FIG. 6

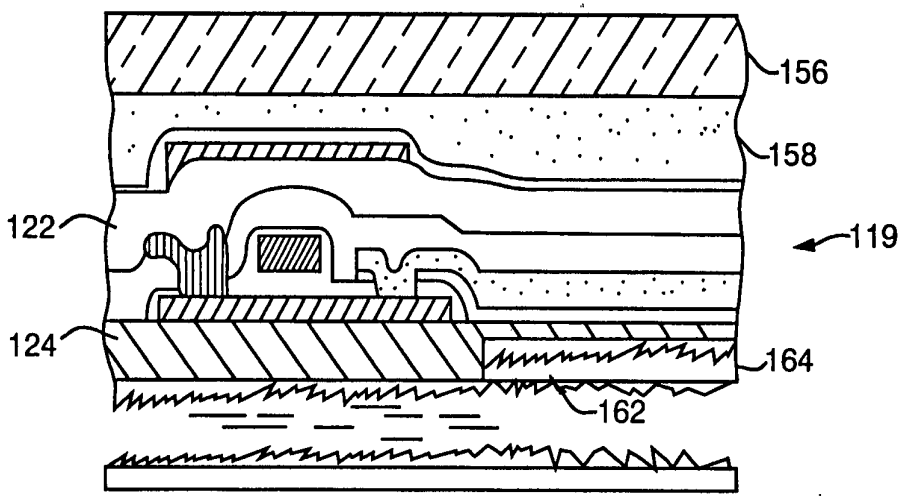
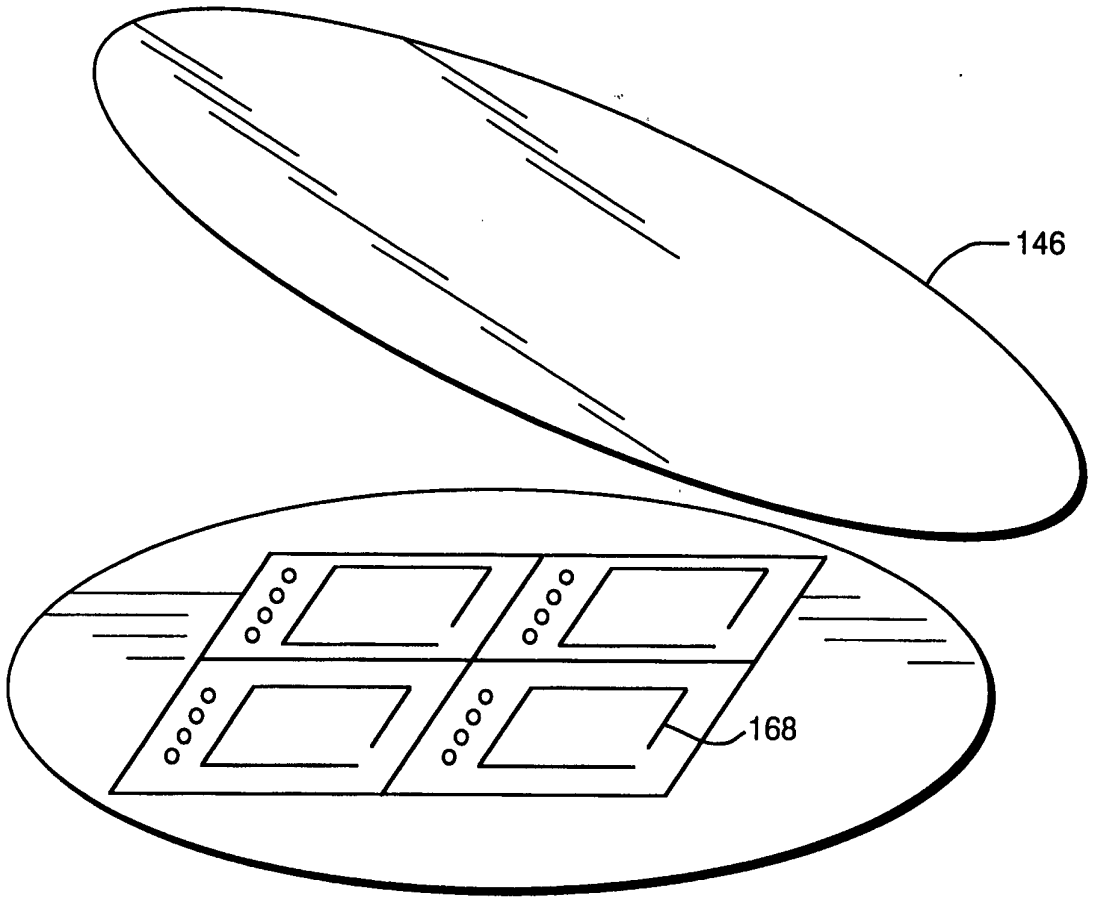


FIG. 7

FIG. 8



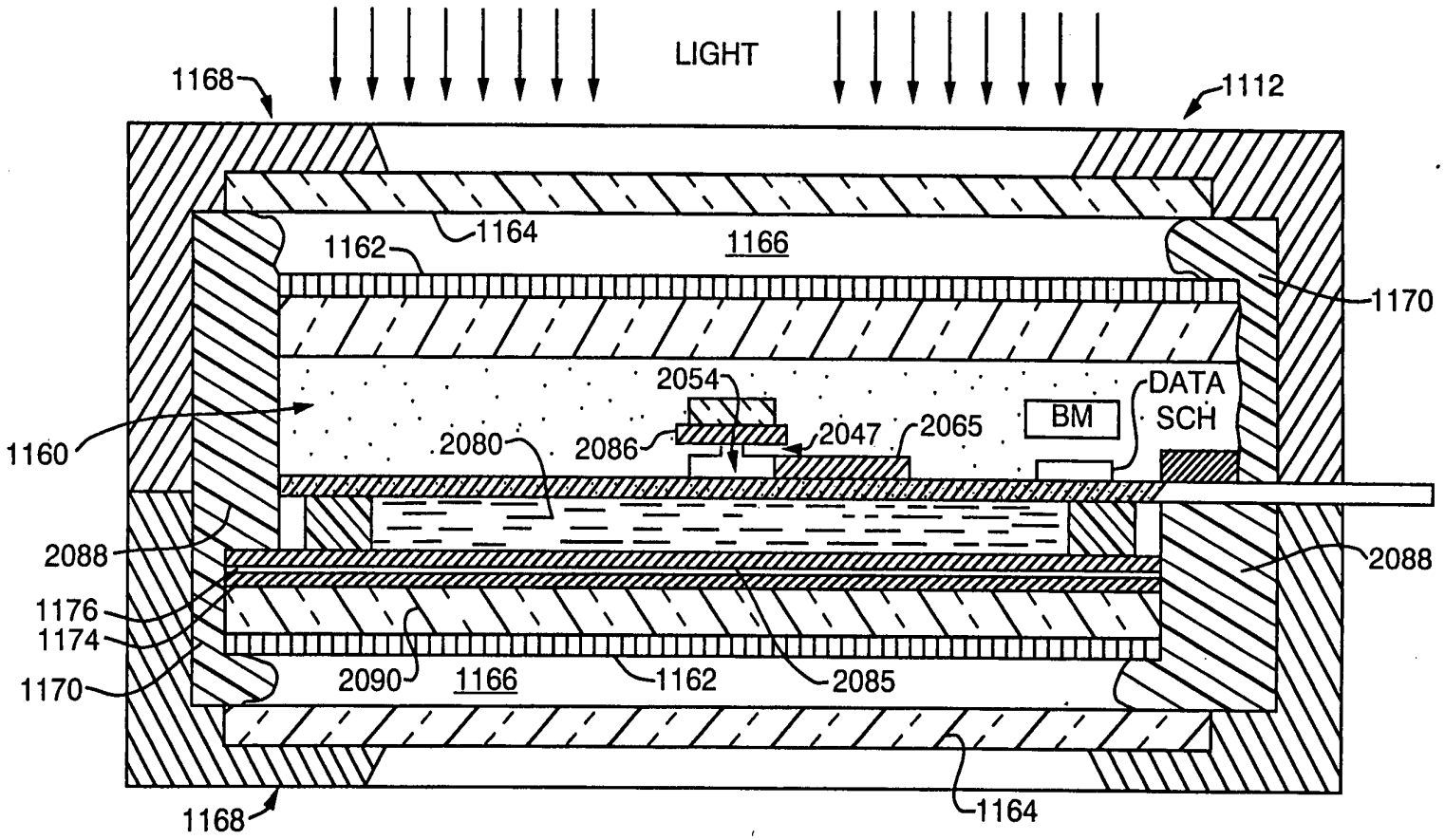


FIG. 9

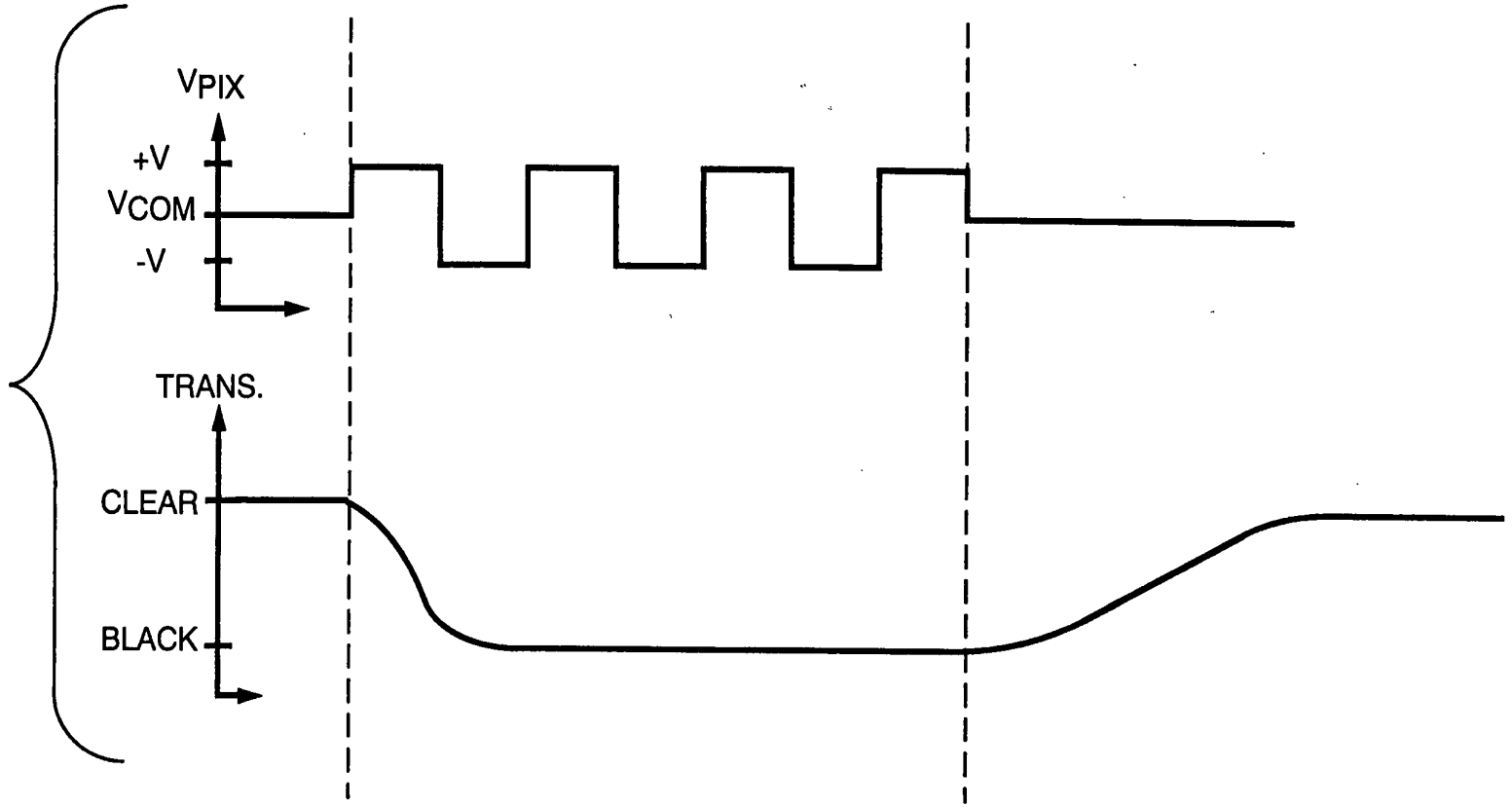


FIG. 10

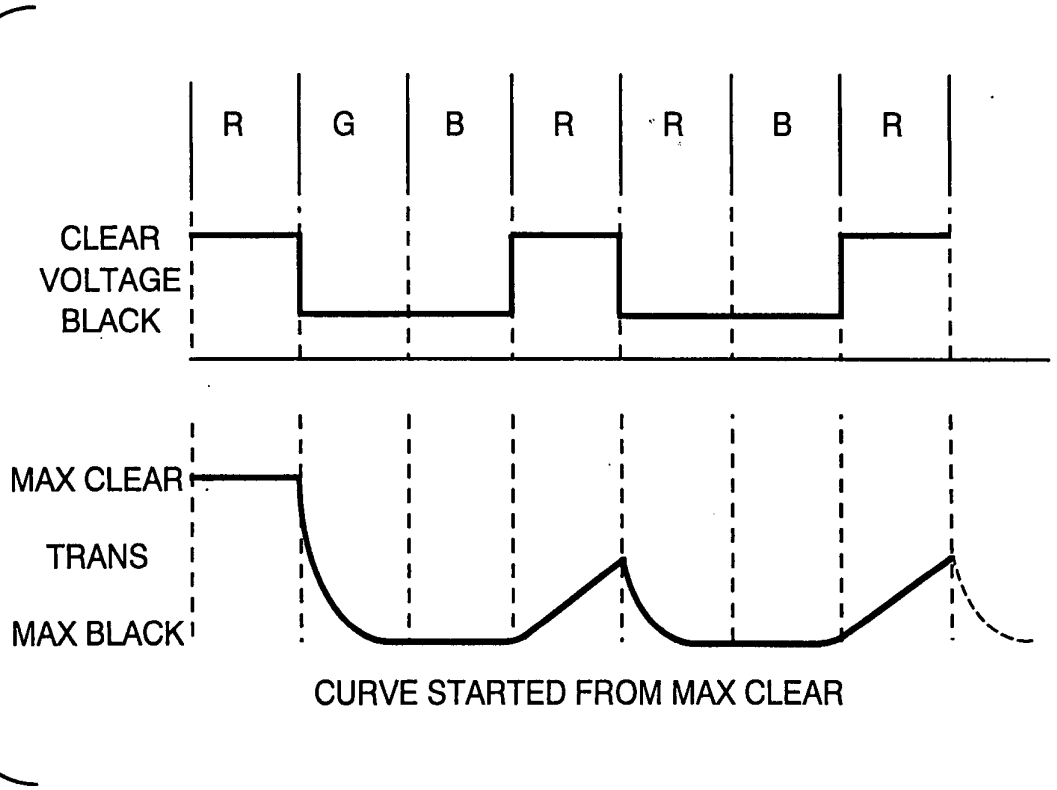


FIG. 11A

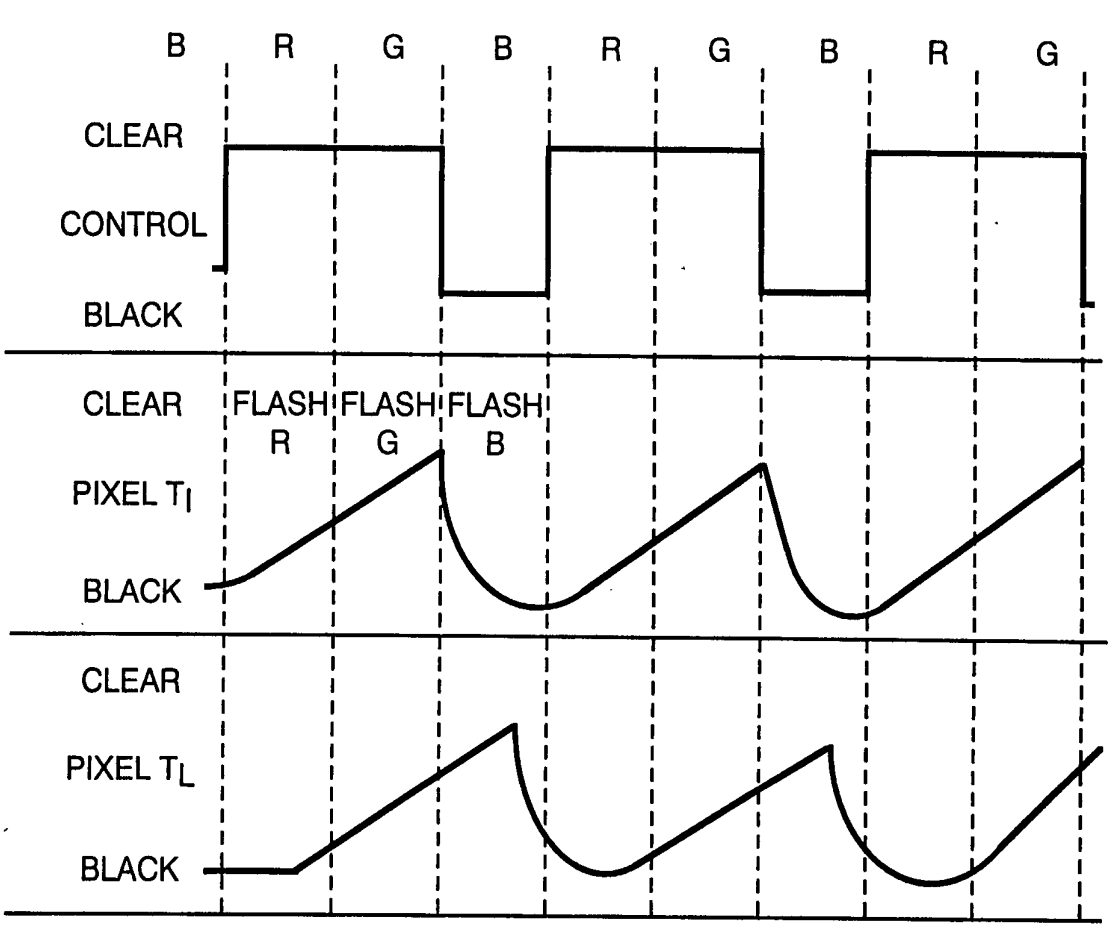


FIG. 11B

• PIXEL T_L IS DELAYED BY 3ms BECAUSE OF WRITE TIME

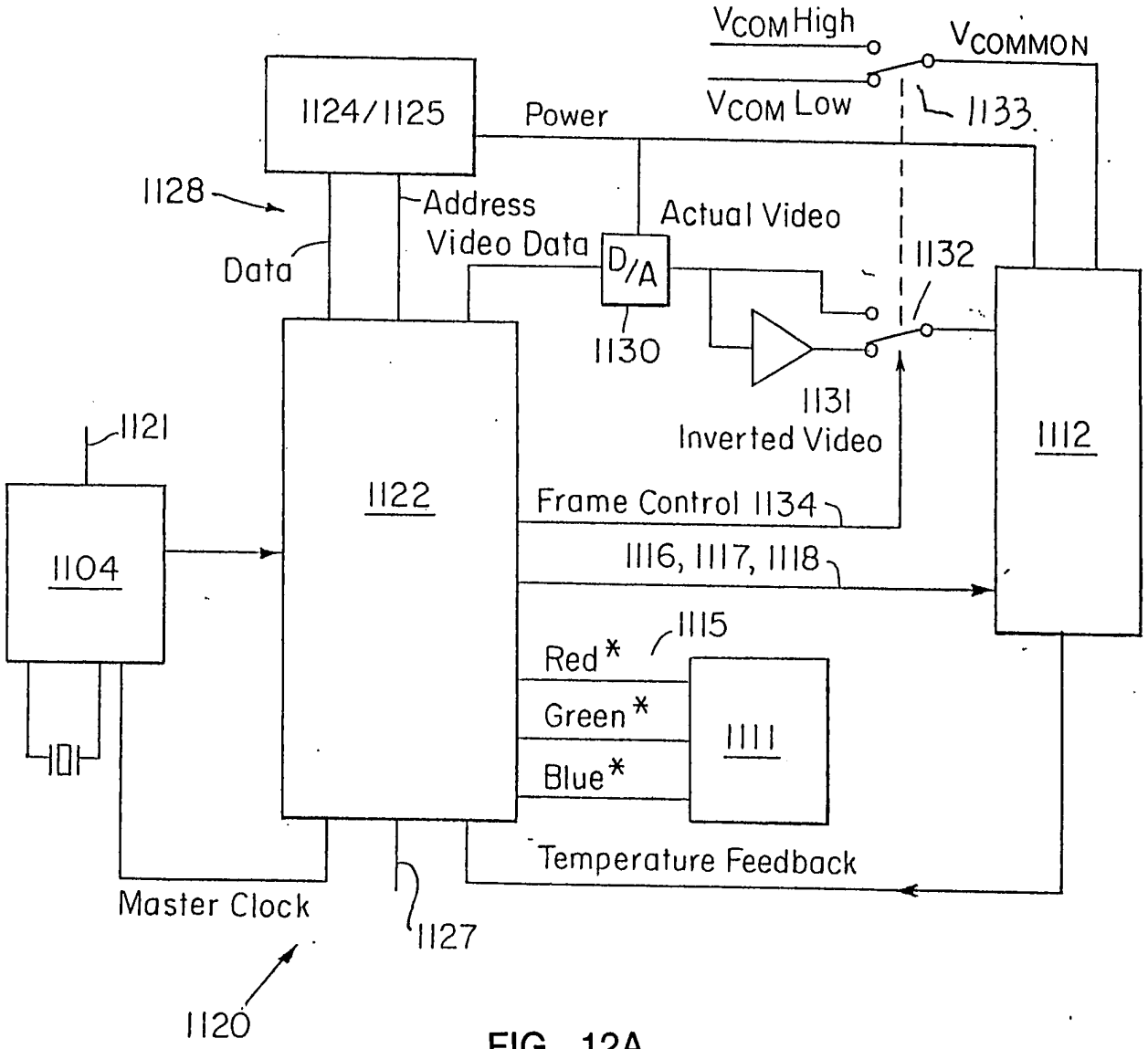


FIG. 12A

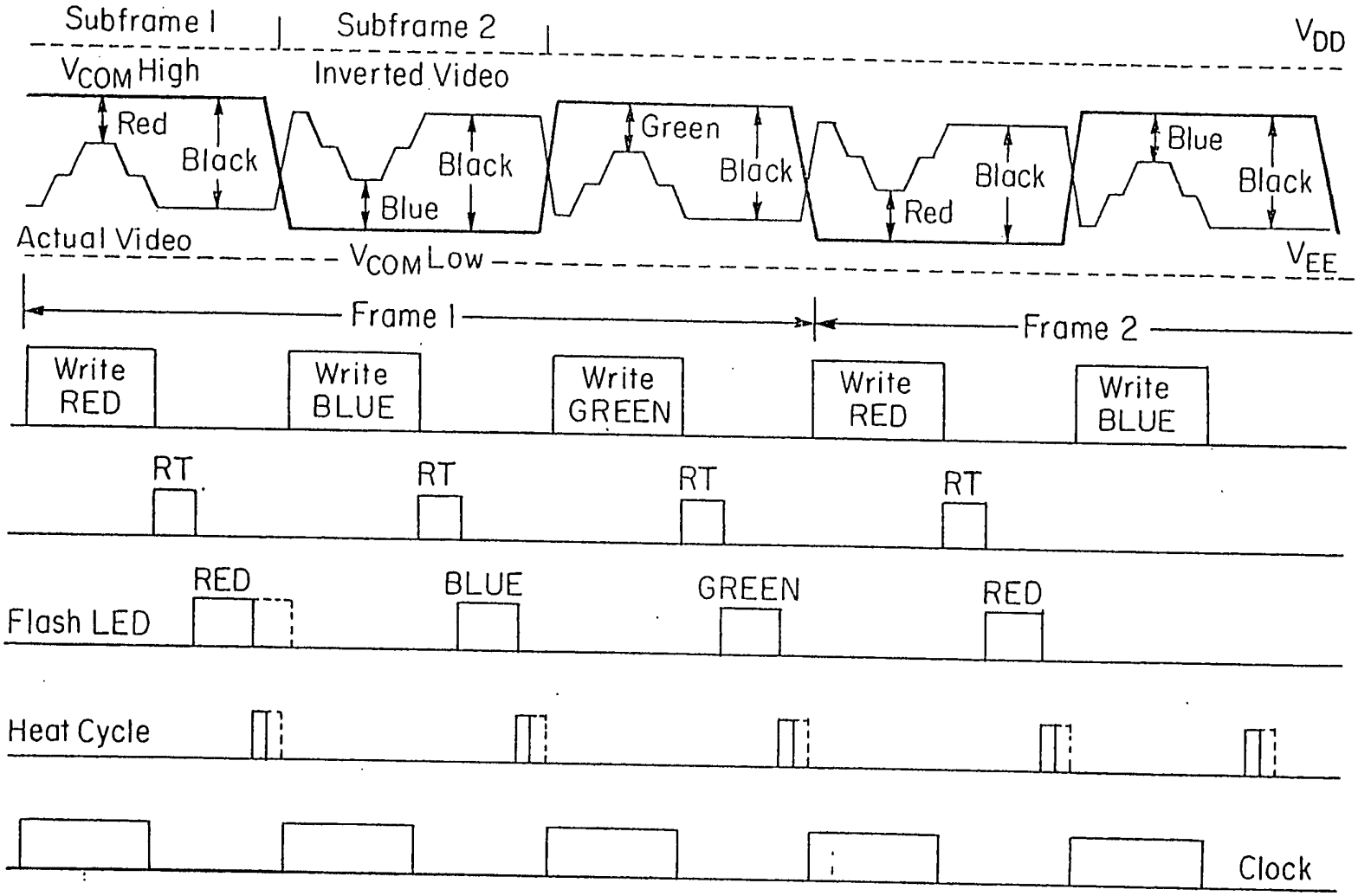


FIG. 12B

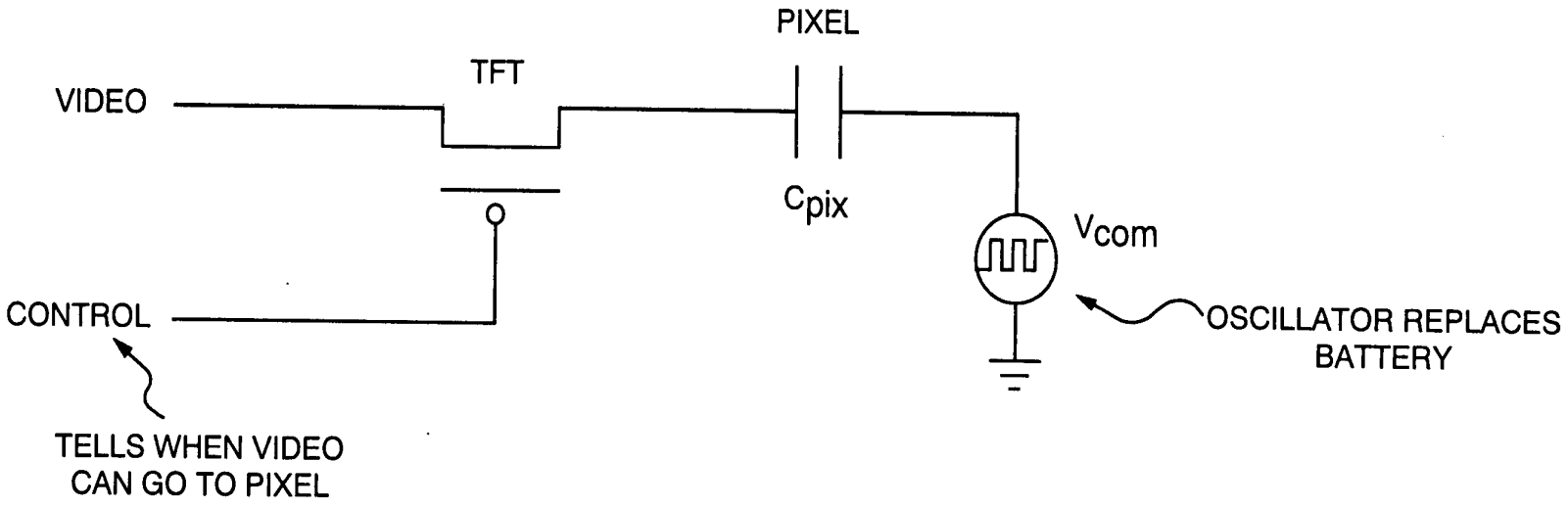


FIG. 12C

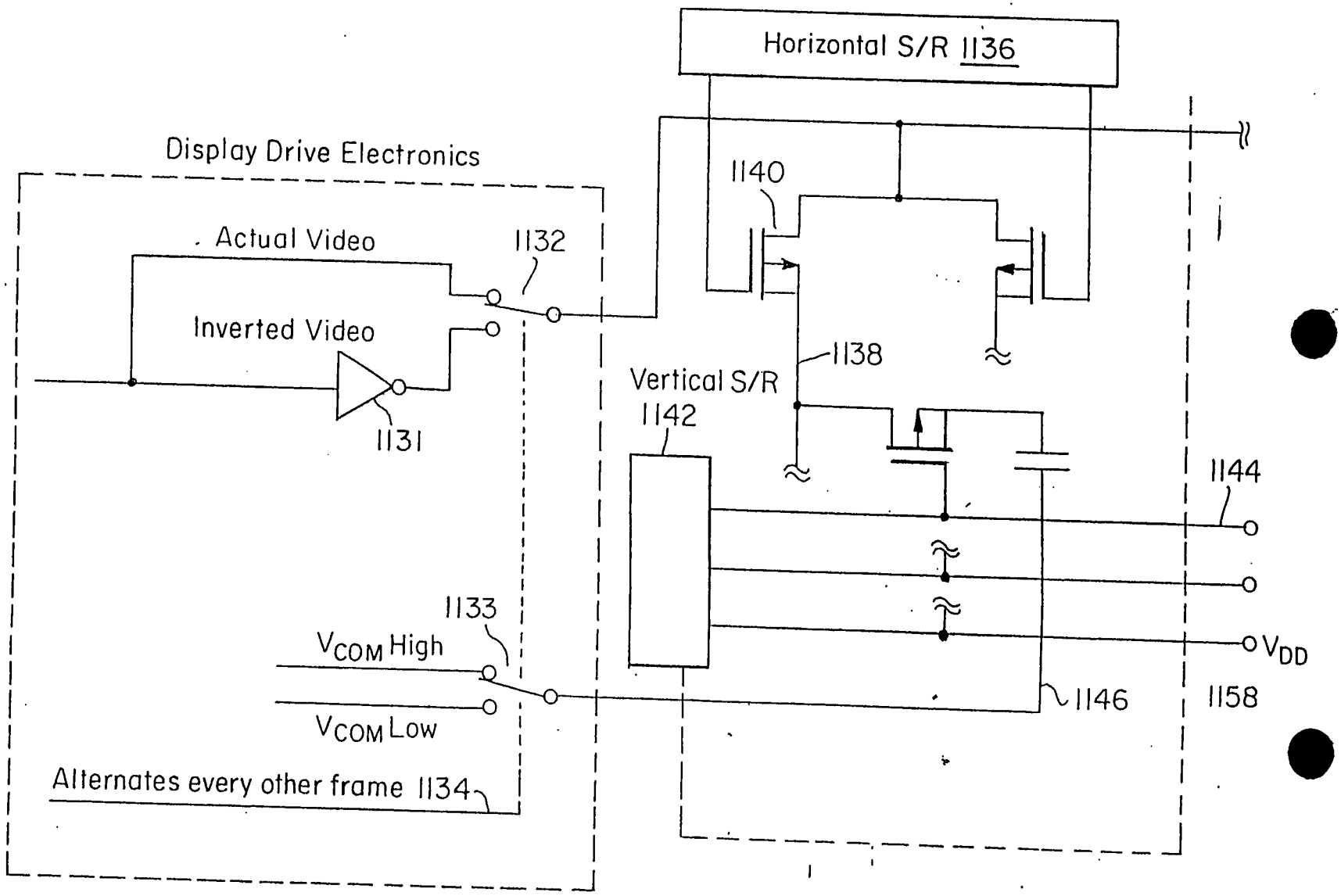


FIG. 12D

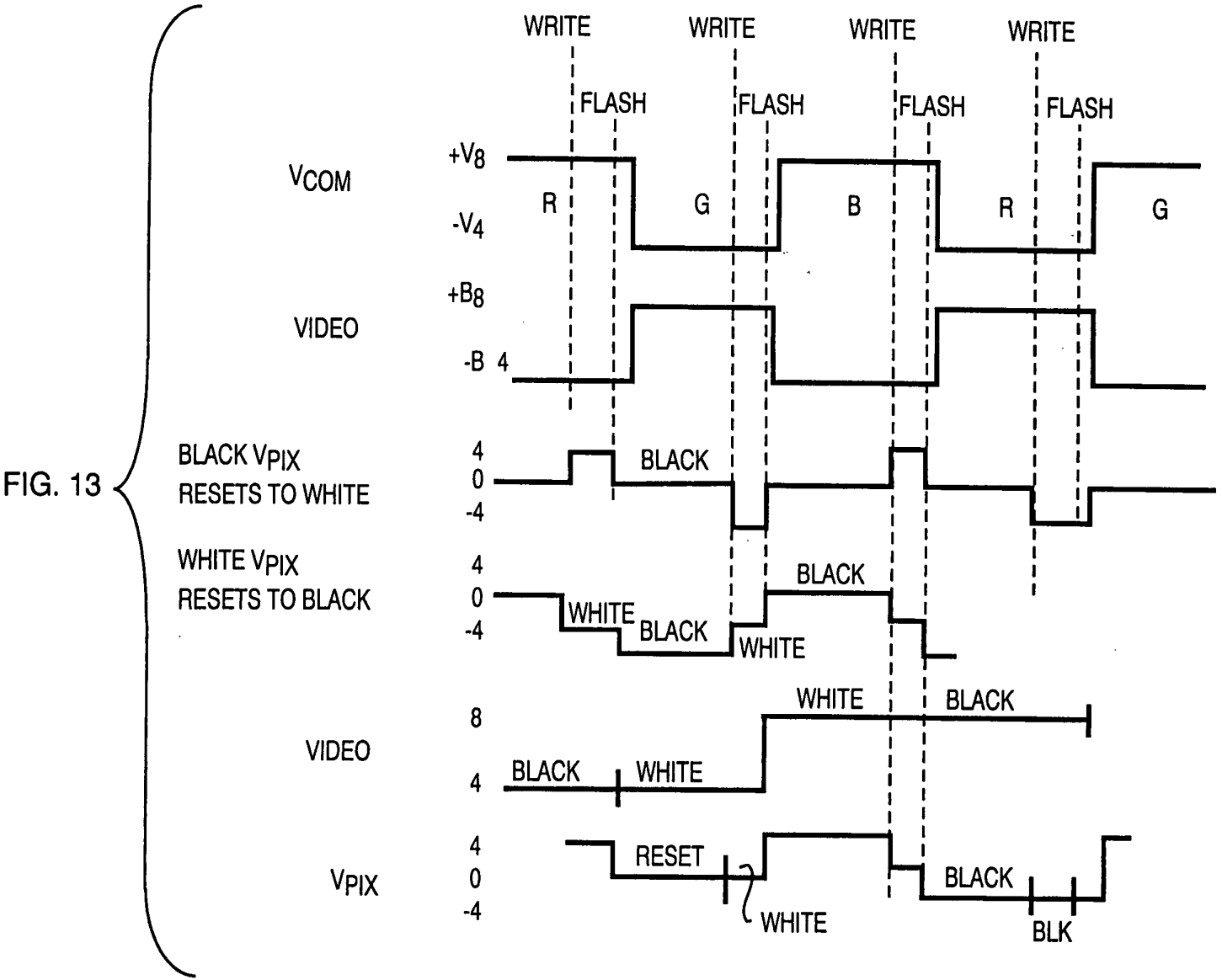


FIG. 13

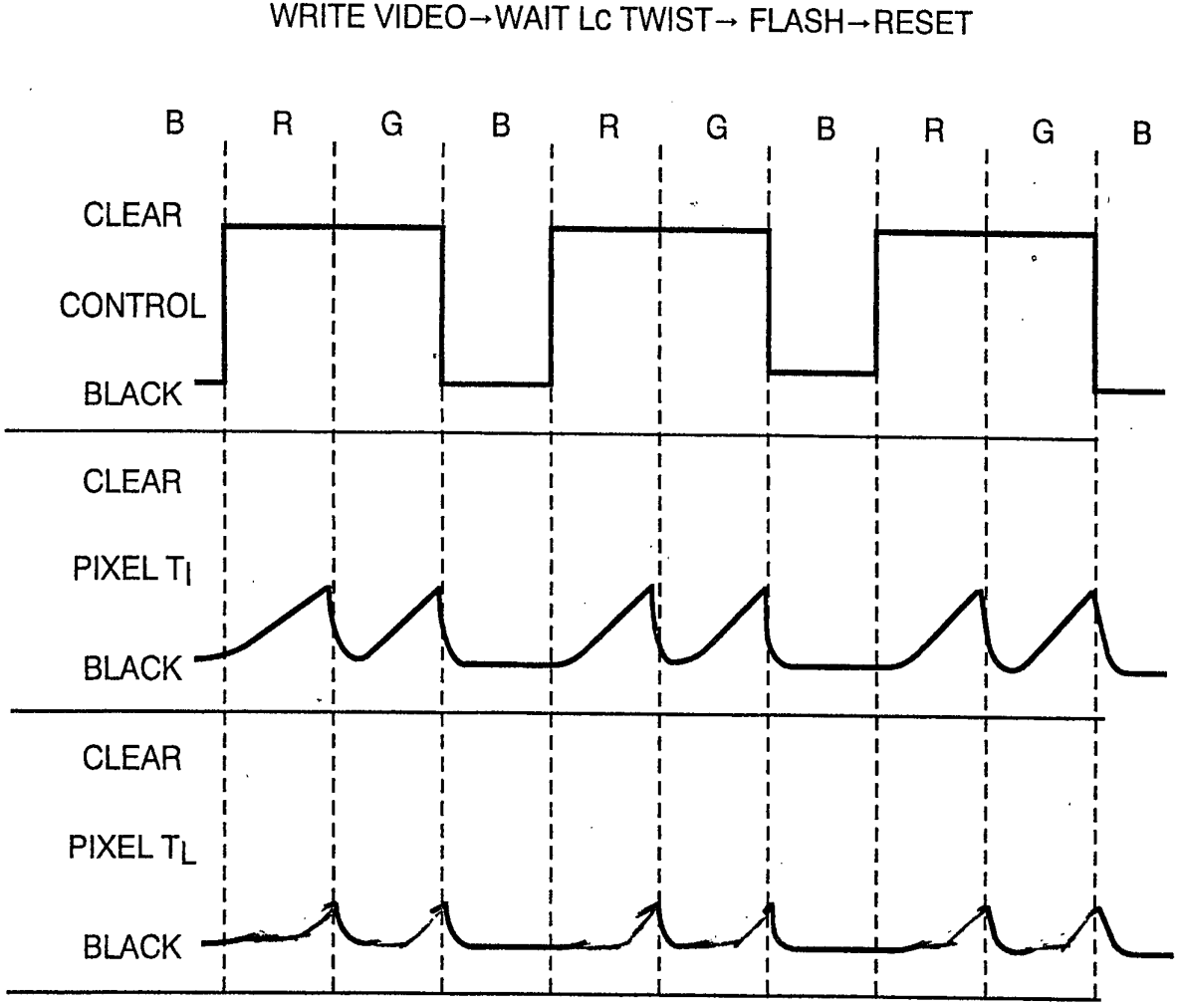


FIG. 14A

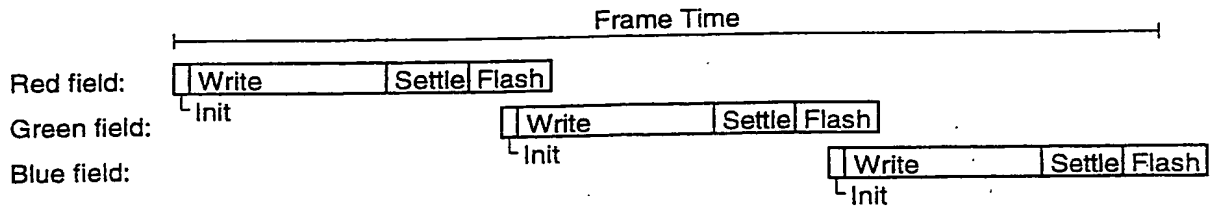


FIG. 14B

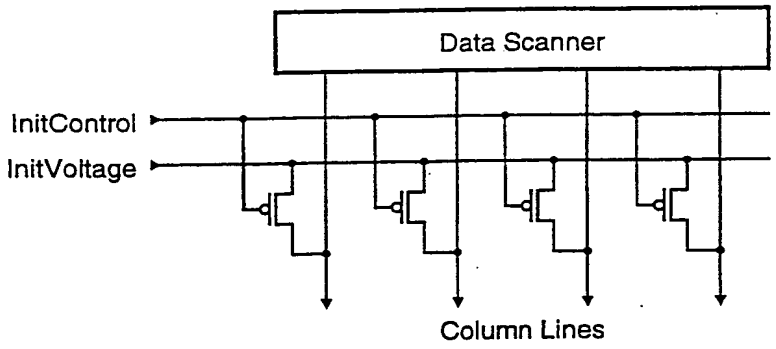


FIG. 14C

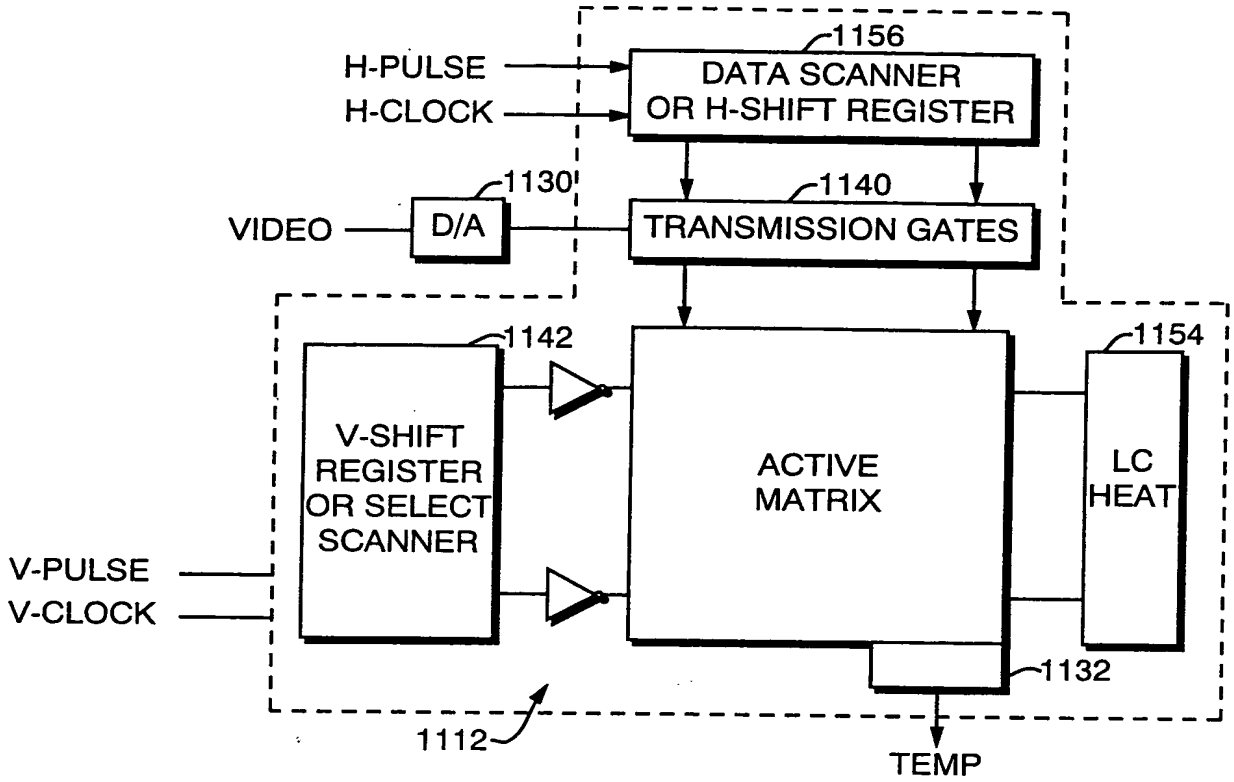


FIG. 15A

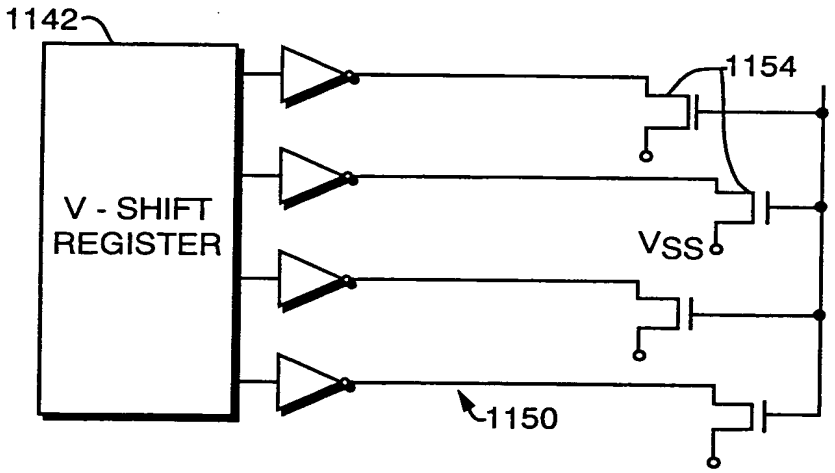


FIG. 15B

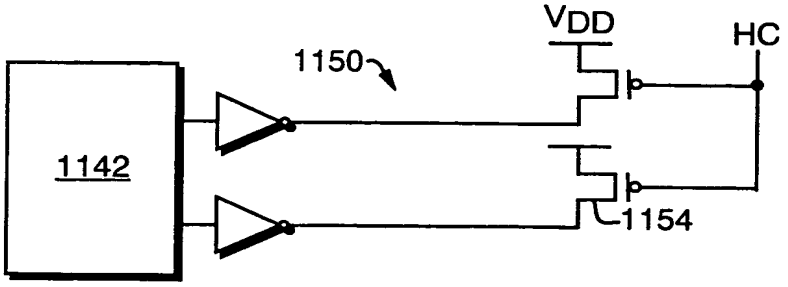


FIG. 15C

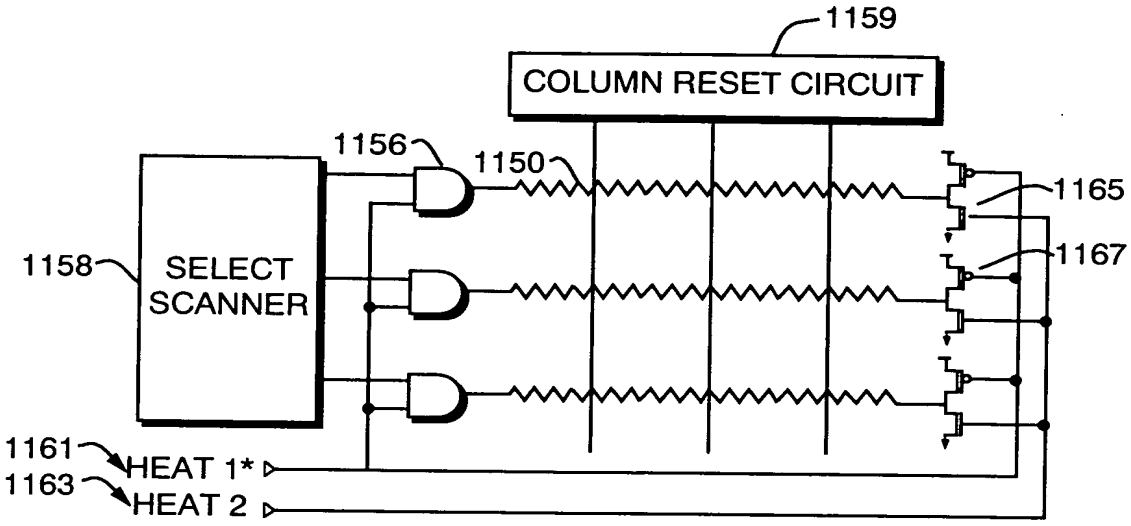


FIG. 15D

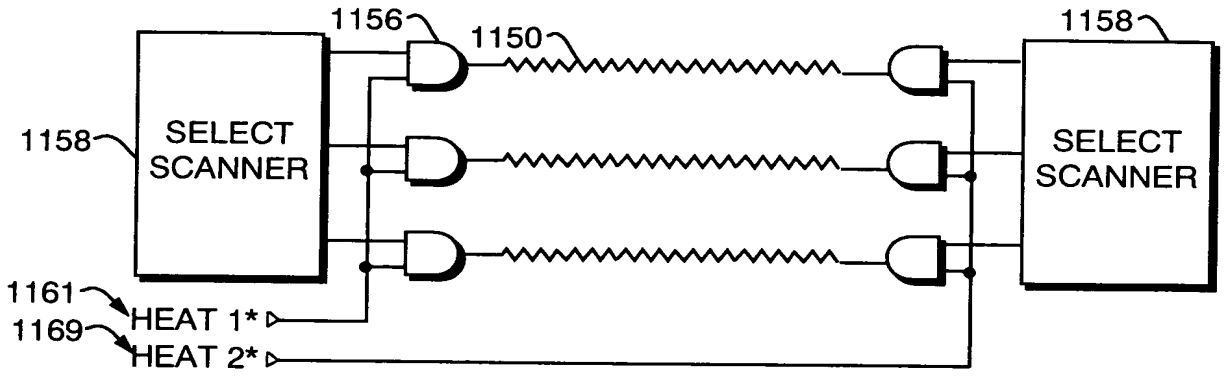


FIG. 15E

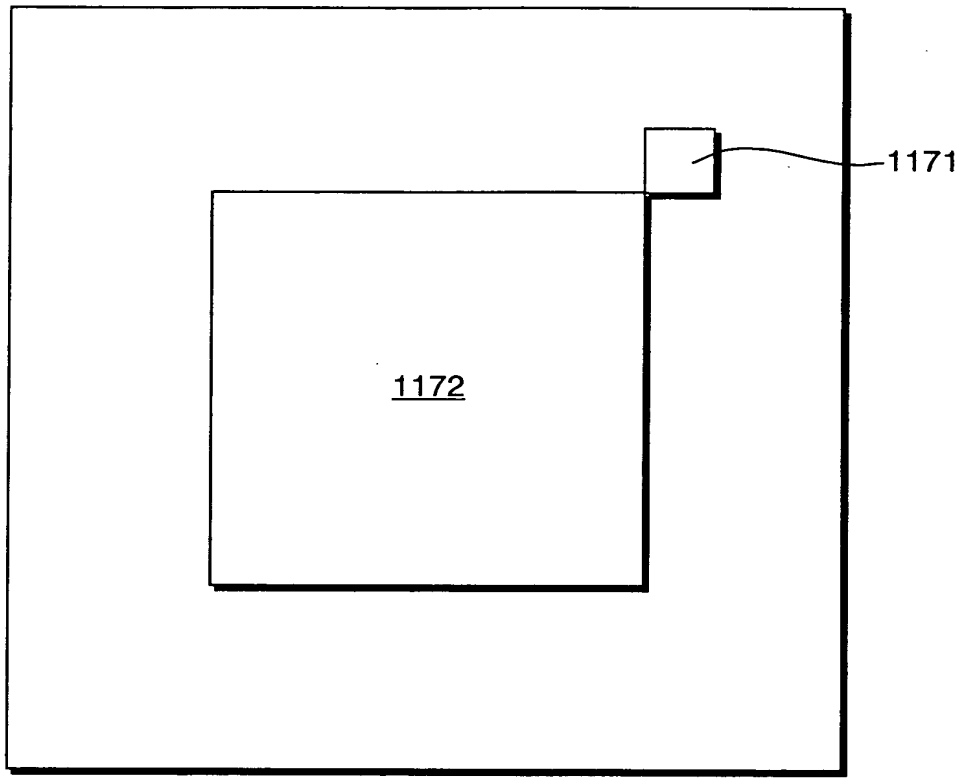


FIG. 15F

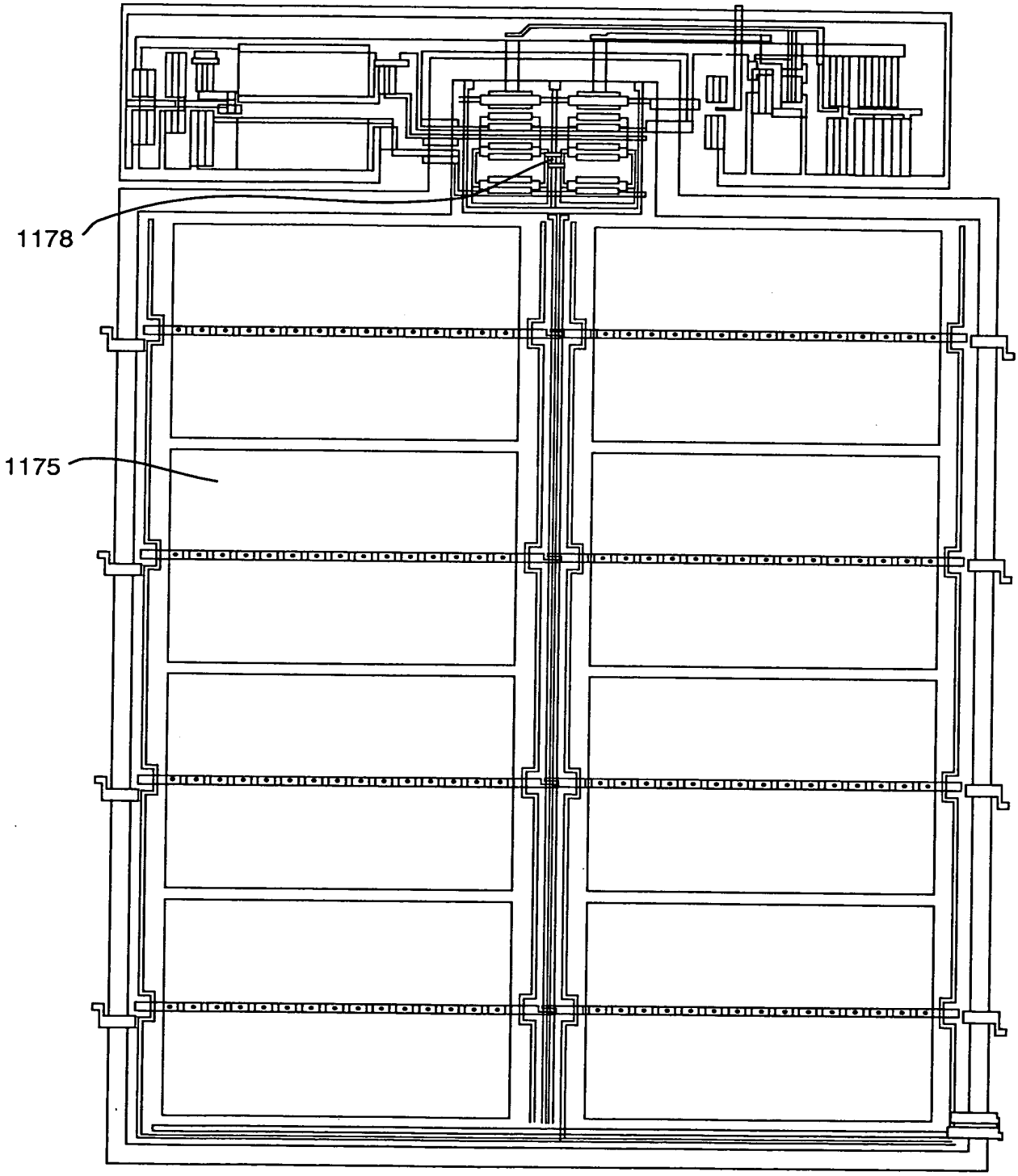


FIG. 15G

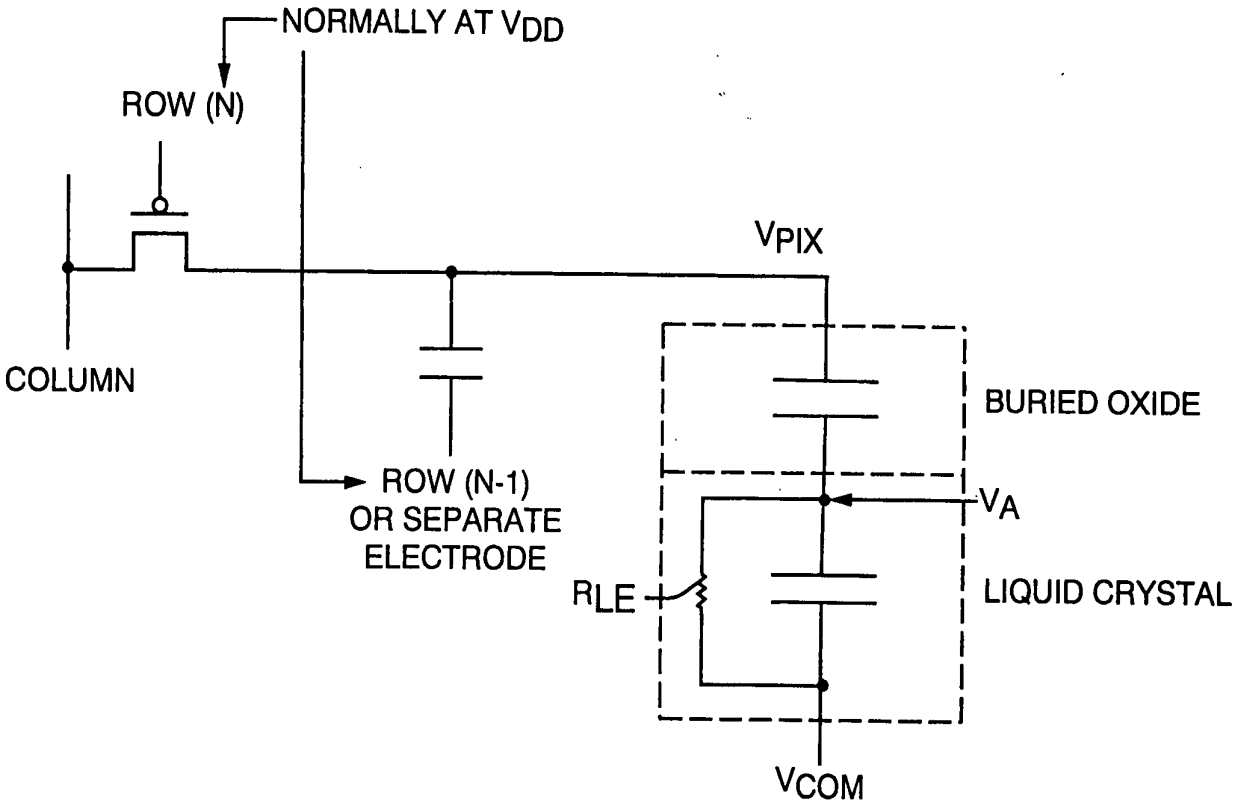
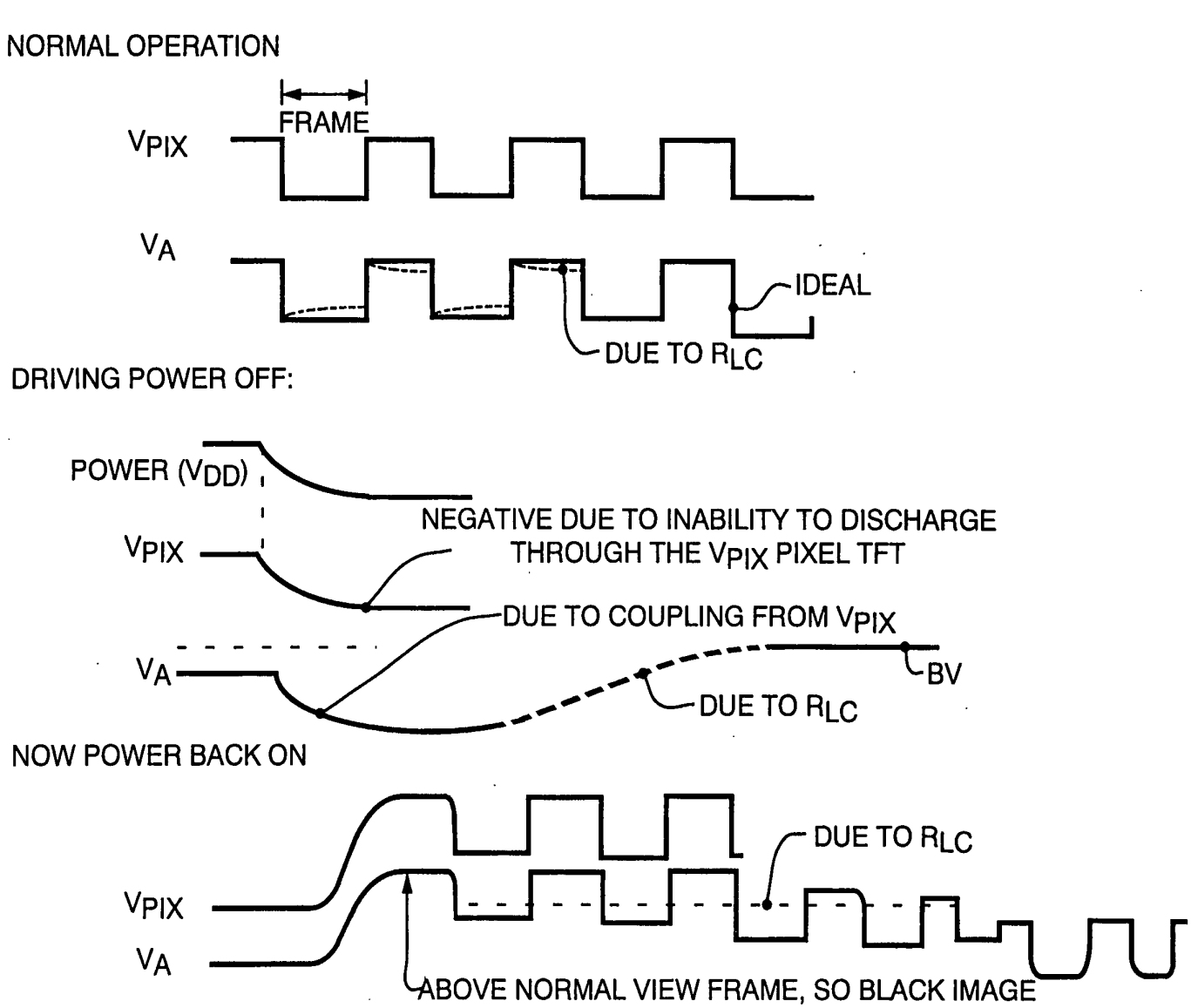


FIG. 16

FIG. 17



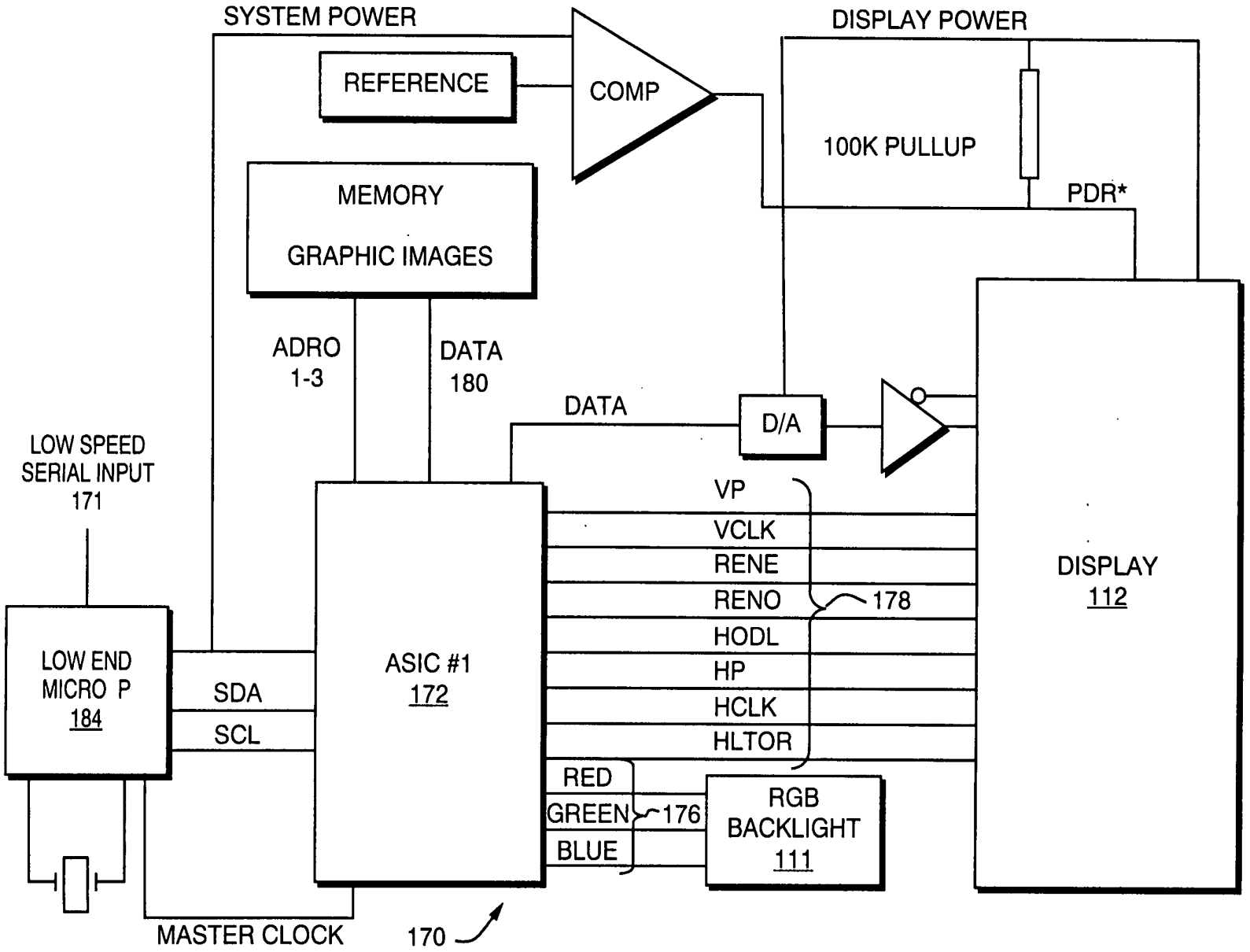


FIG. 18

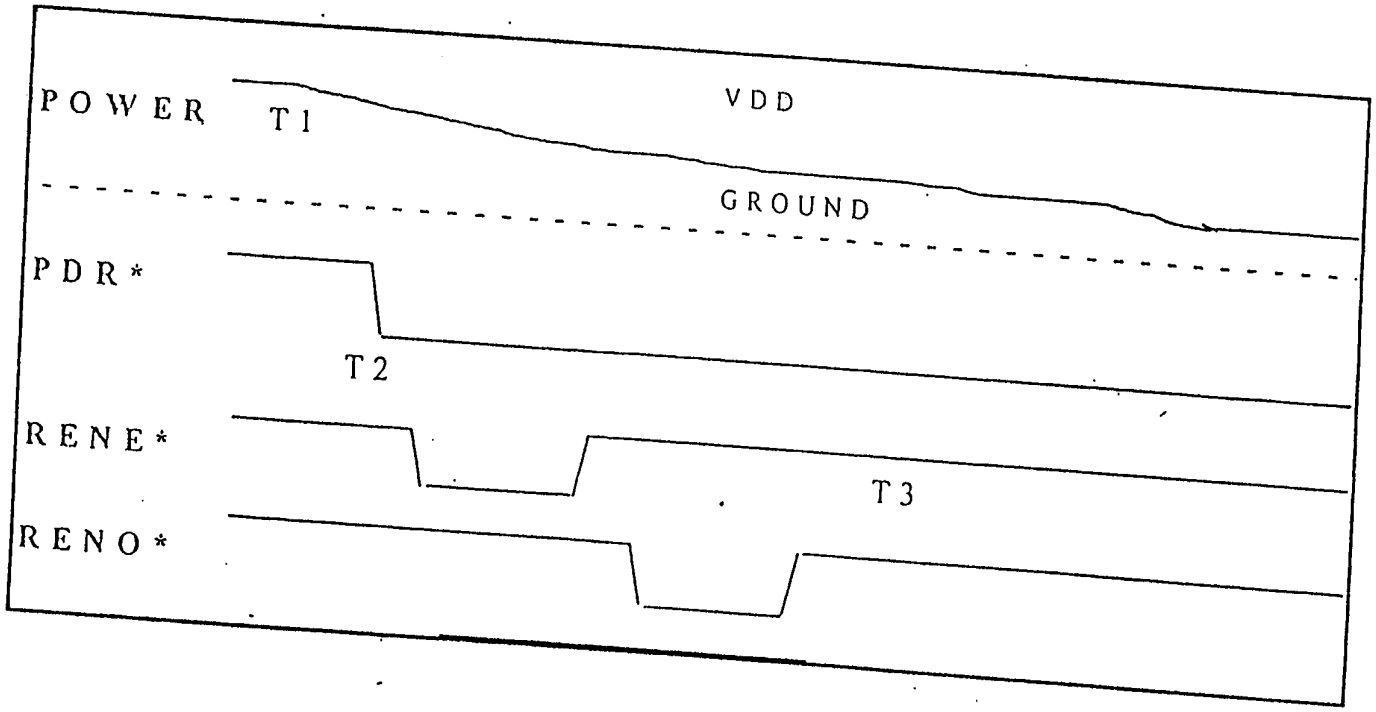


FIG. 19A

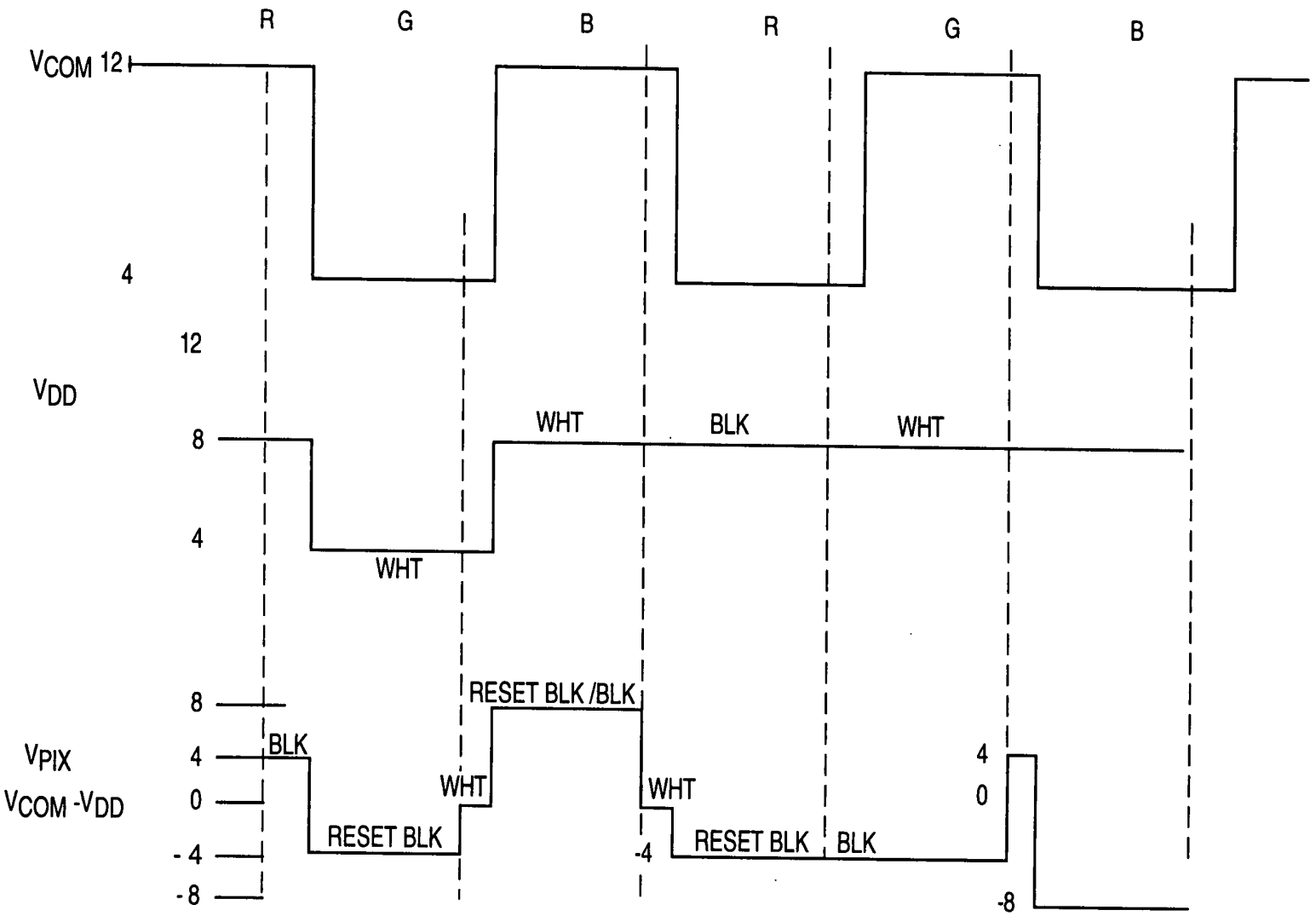
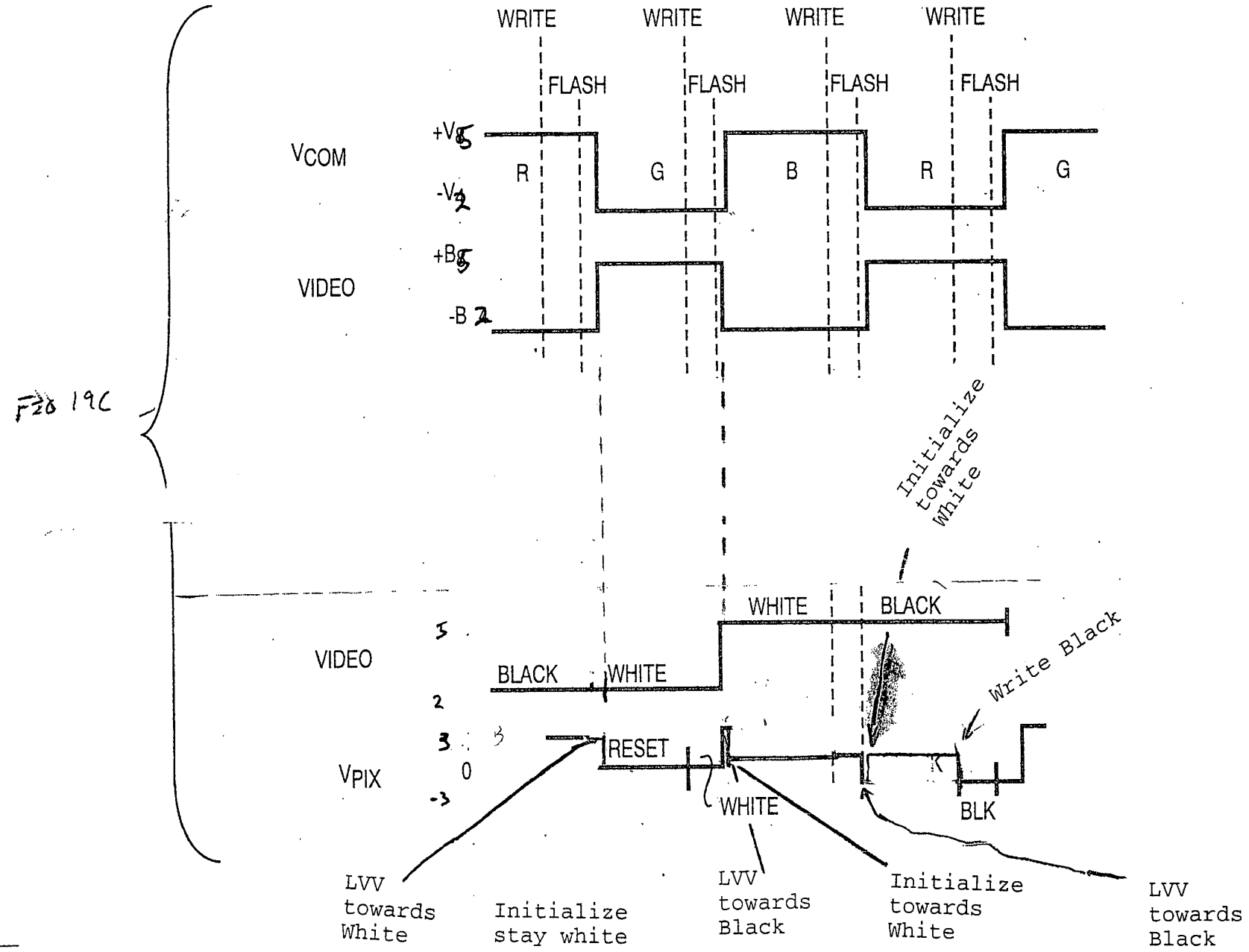


FIG. 19B


WRITE
WRITE
WRITE
WRITE
FLASH
FLASH
FLASH
FLASH
VCOM
+V
-V
R
G
B
R
G
VIDEO
+B
-B
Initialize towards White
WHITE
BLACK
VIDEO
5
BLACK
WHITE
Write Black
2
3
RESET
VPIX
0
-3
WHITE
BLK
LVV towards White
Initialize stay white
LVV towards Black
Initialize towards White
LVV towards Black

F28 19C

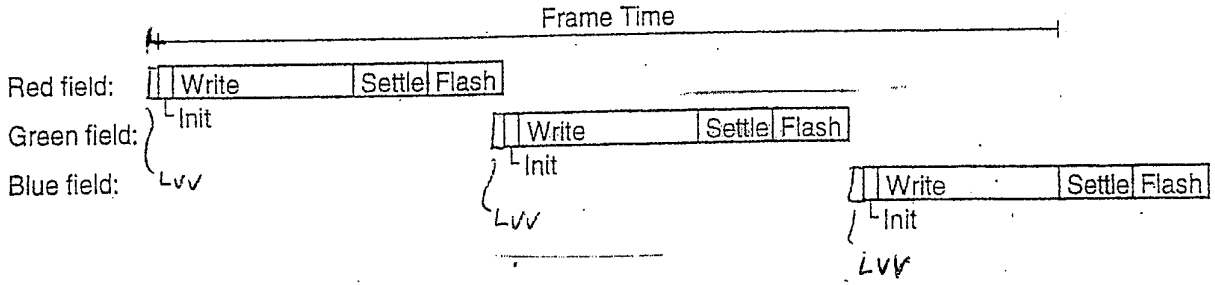


FIG 19D

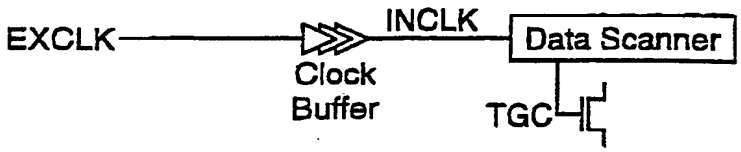


FIG. 20A

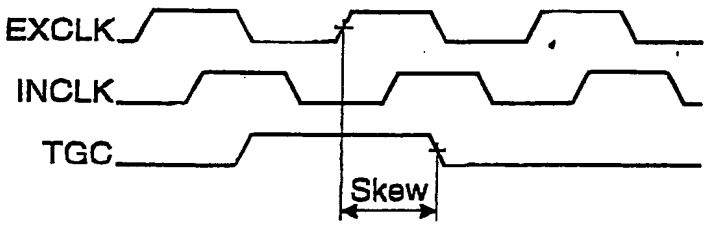


FIG. 20B

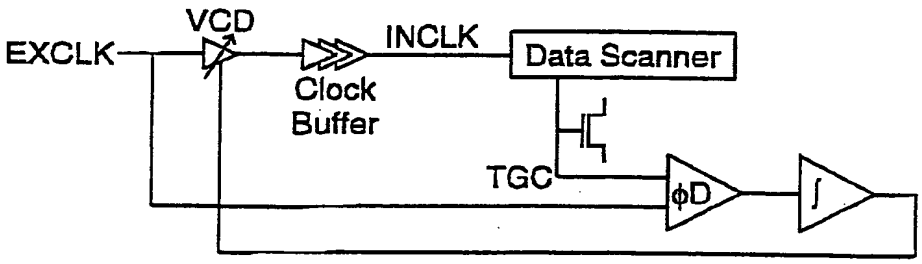


FIG. 20C

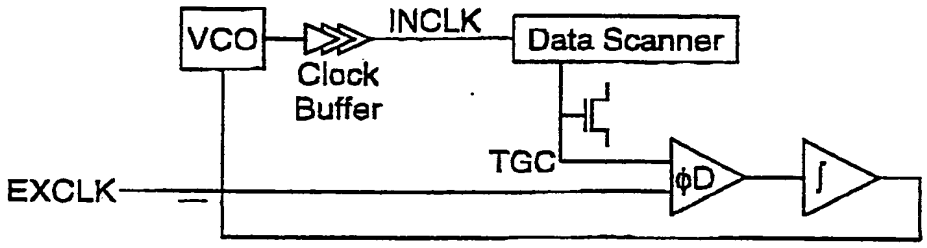


FIG. 20D

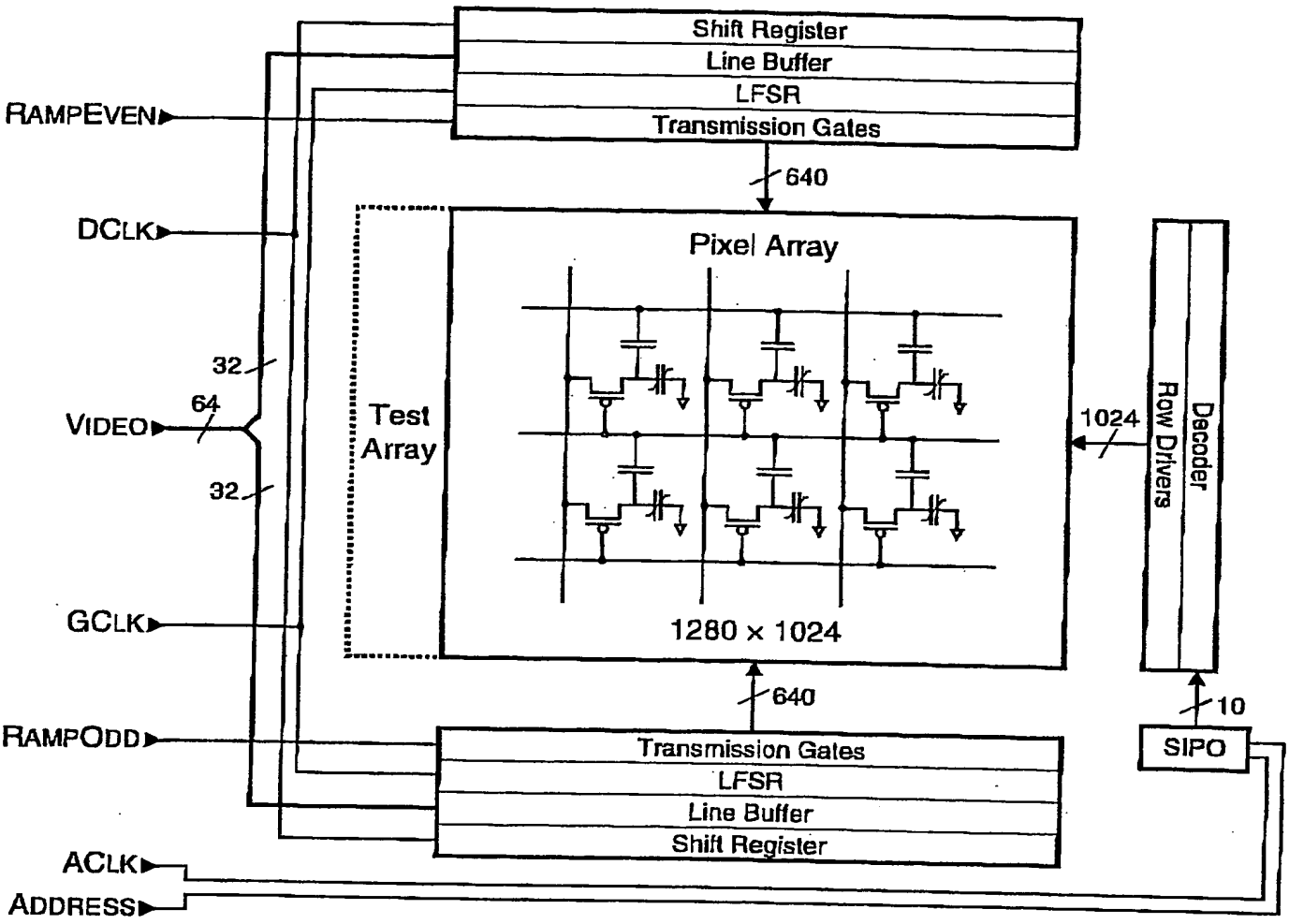

Shift Register
Line Buffer
LFSR
Transmission Gates
RAMPEVEN
640
DCLK
Pixel Array
32
64
VIDEO
32
Test Array
1024
Decoder
Row Drivers
GCLK
1280 x 1024
640
10
SIPO
RAMPODD
Transmission Gates
LFSR
Line Buffer
Shift Register
ACLK
ADDRESS

FIG. 20E

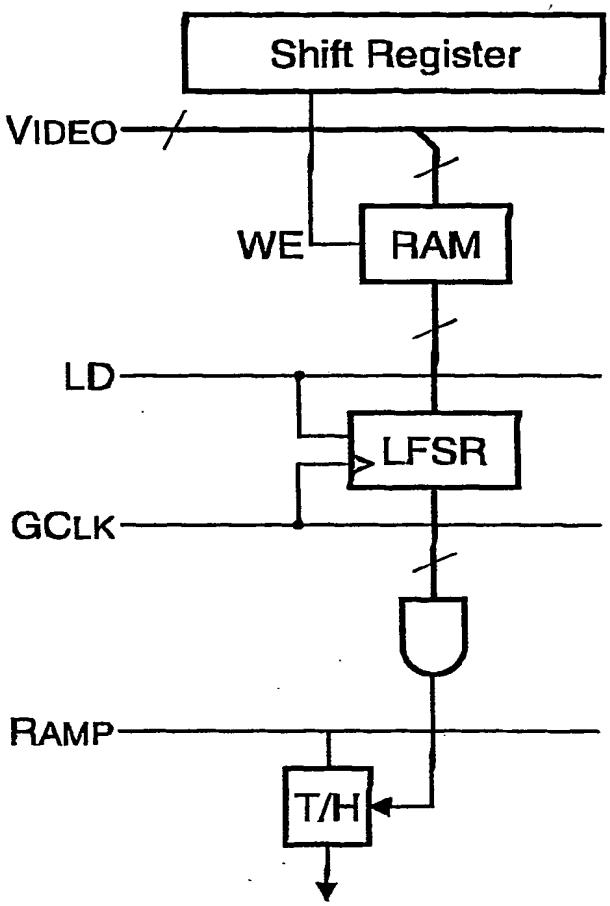


FIG. 20F

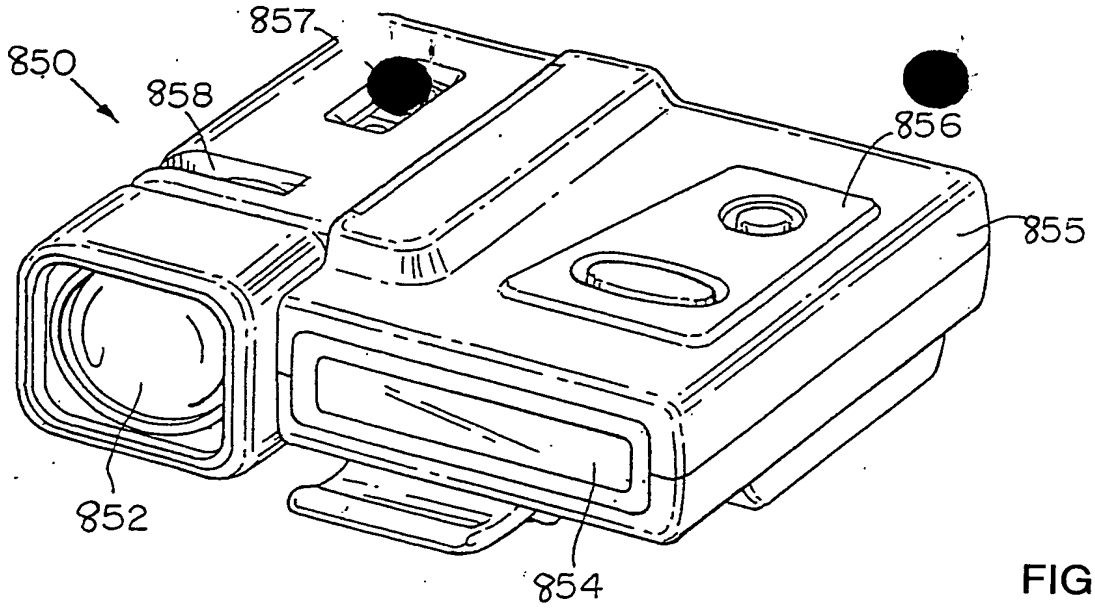
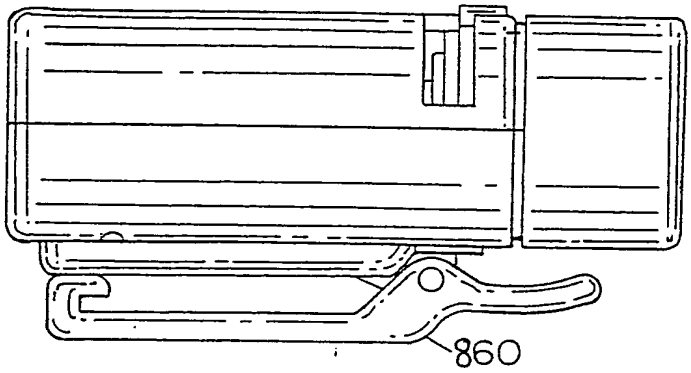


FIG. 21A

FIG. 21C



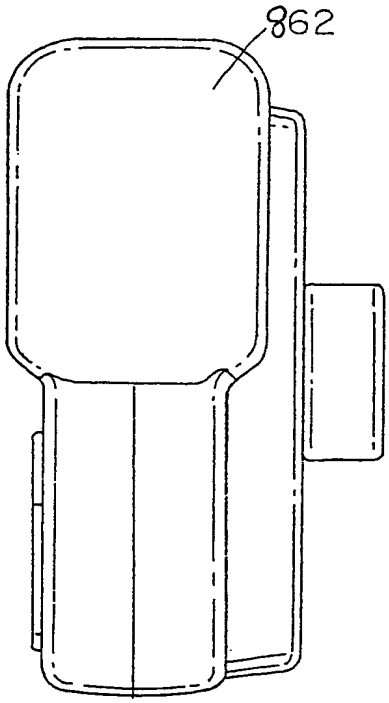


FIG. 21B

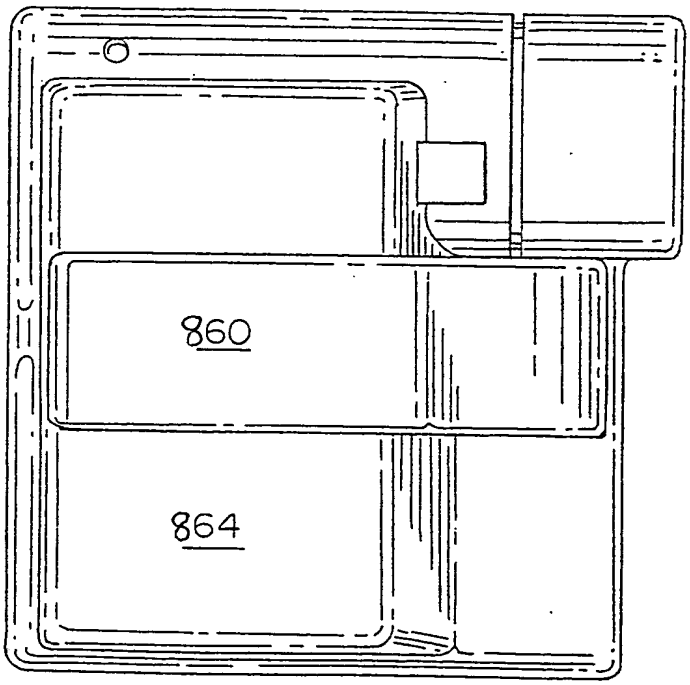


FIG. 21D

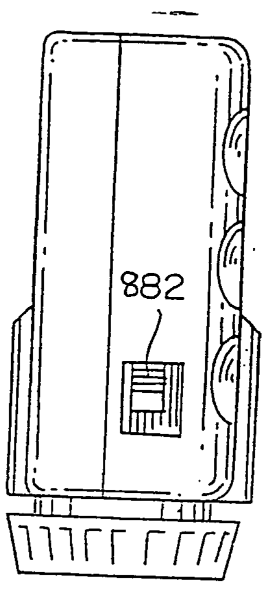


FIG. 21G

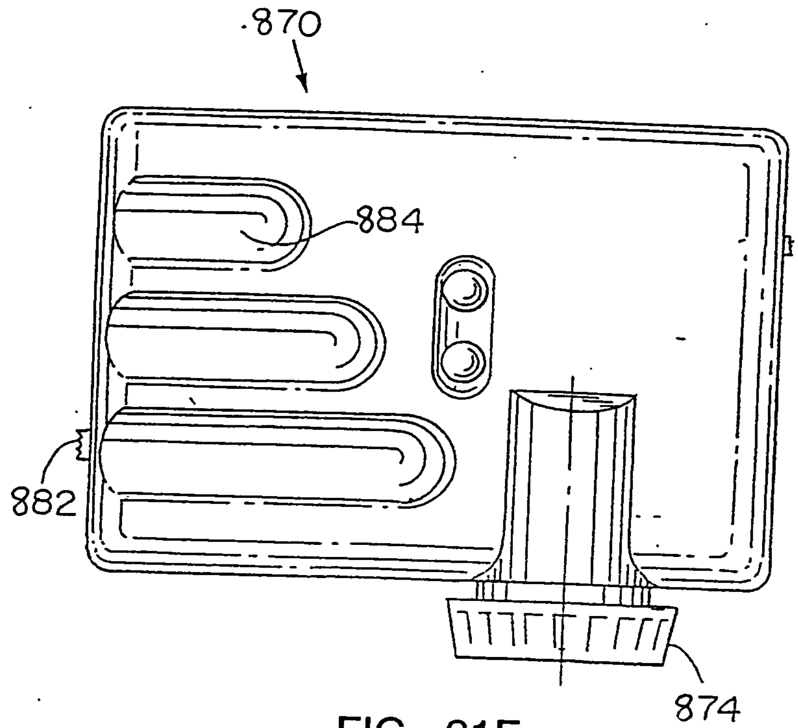


FIG. 21F

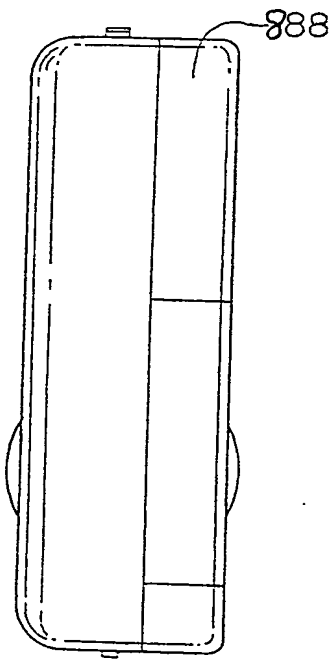


FIG. 21H

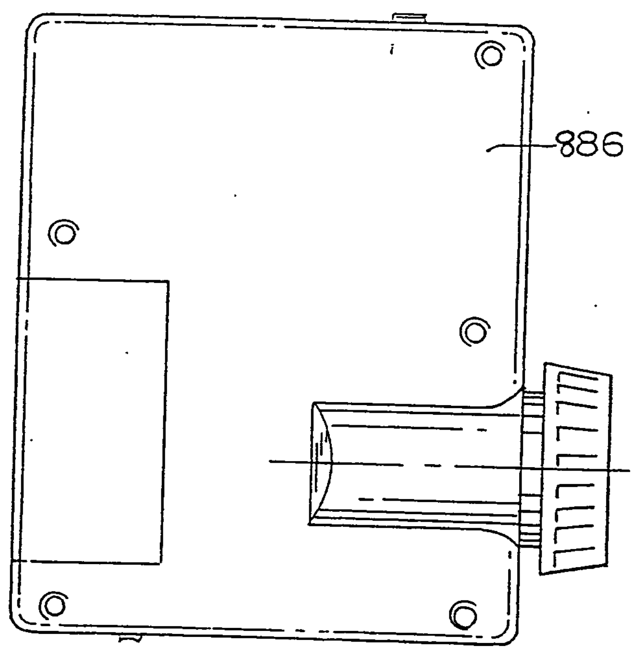
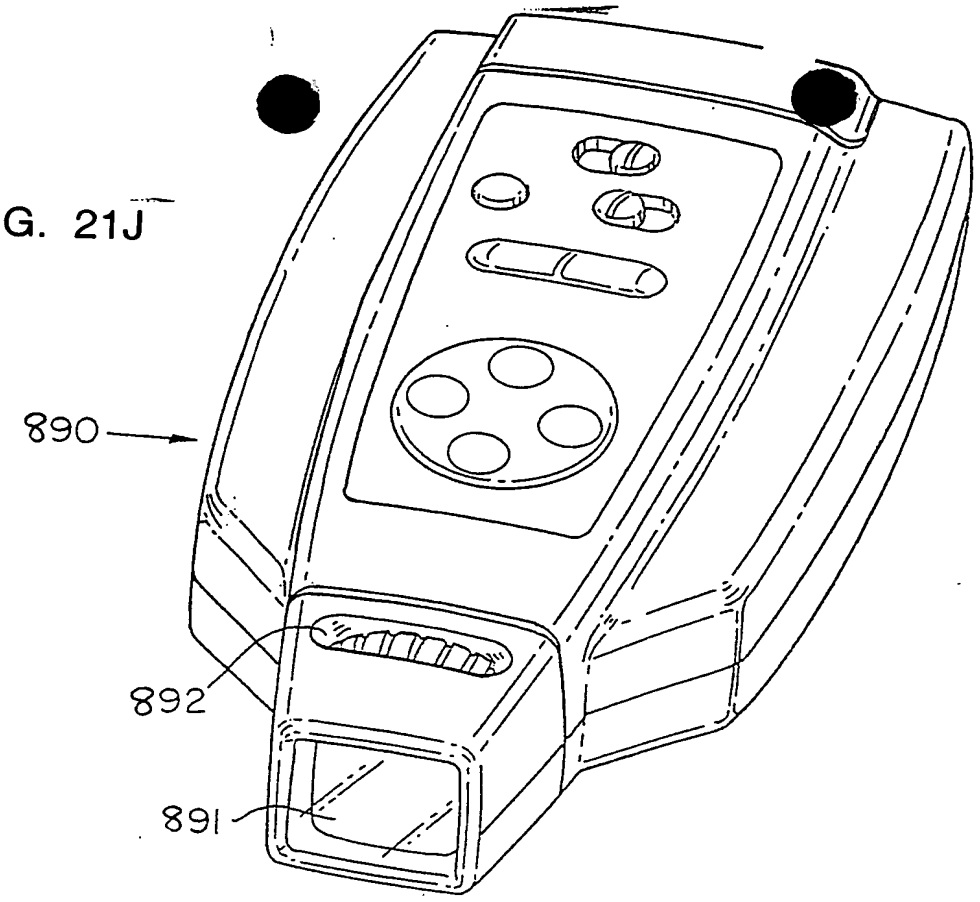


FIG. 21I

FIG. 21J



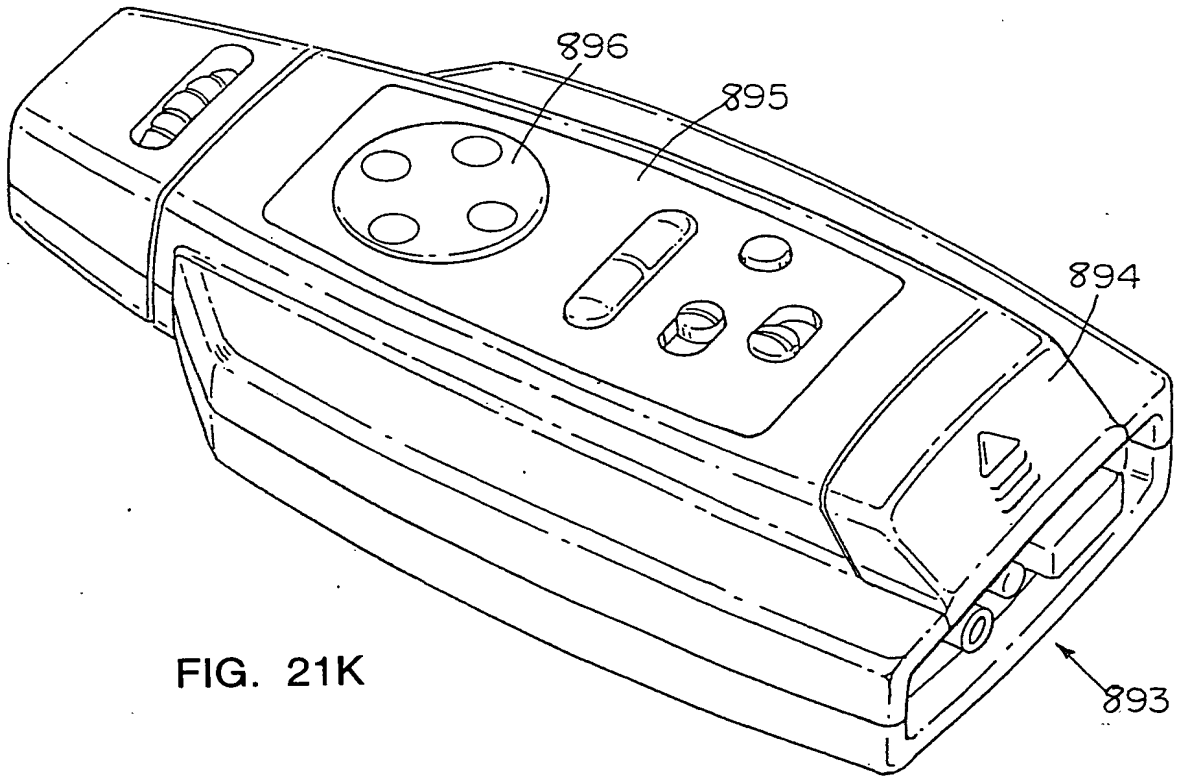


FIG. 21K

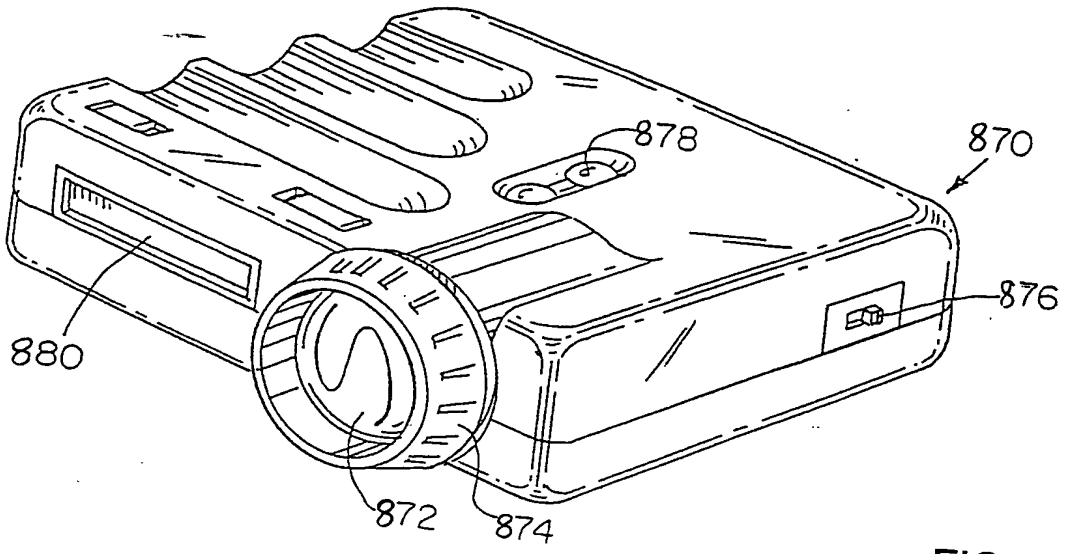


FIG. 21E

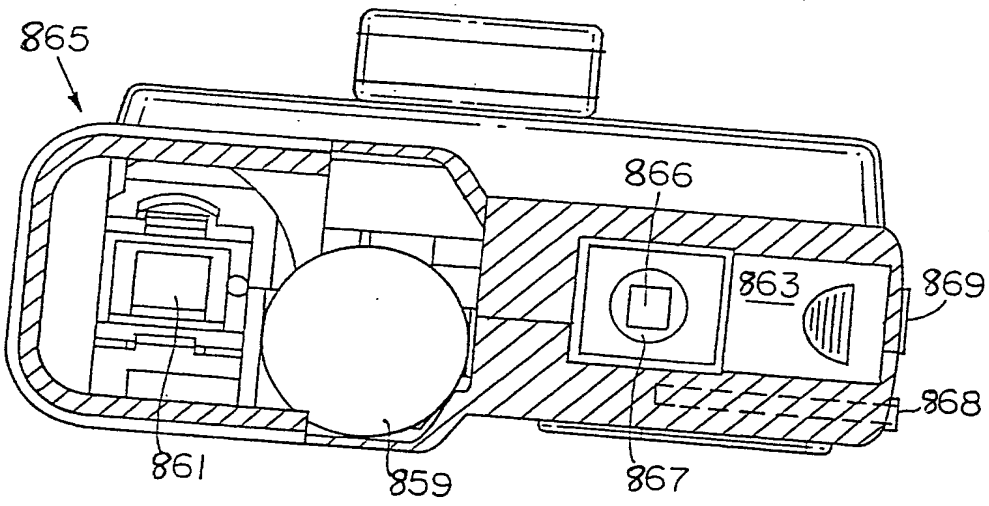


FIG. 22

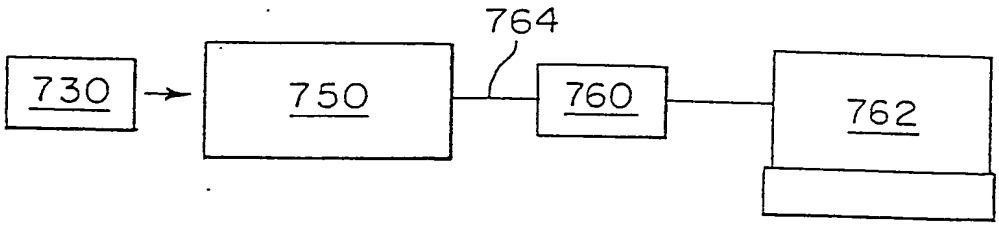


FIG. 23A

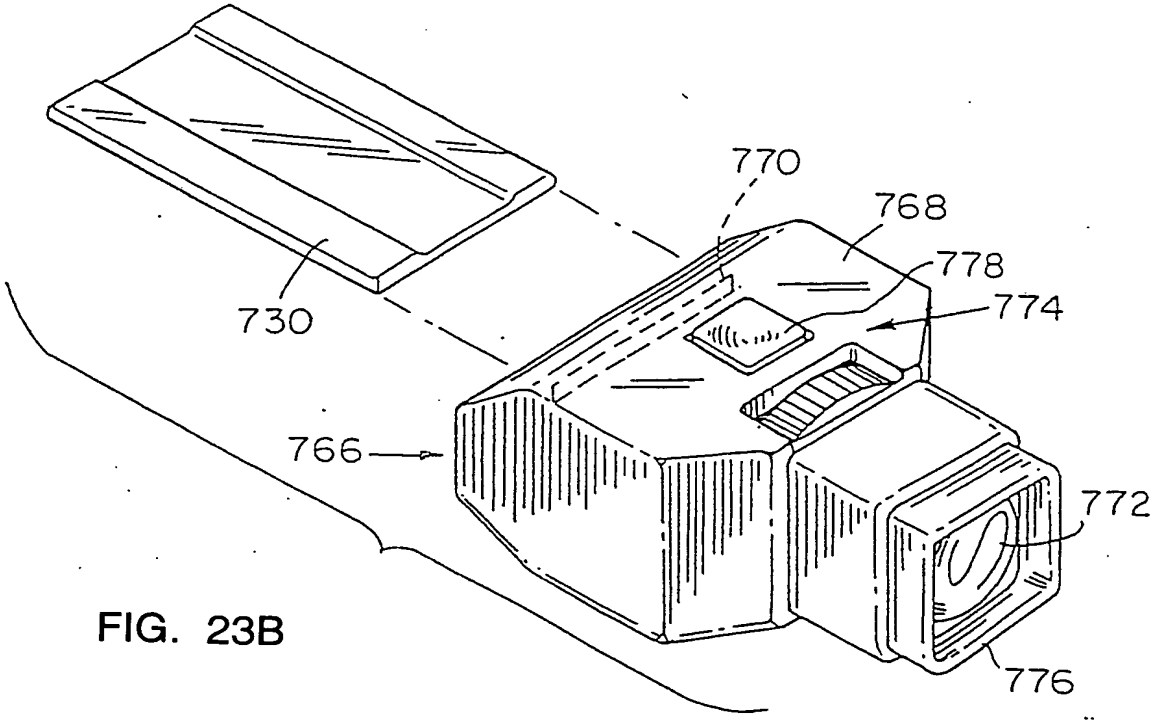


FIG. 23B

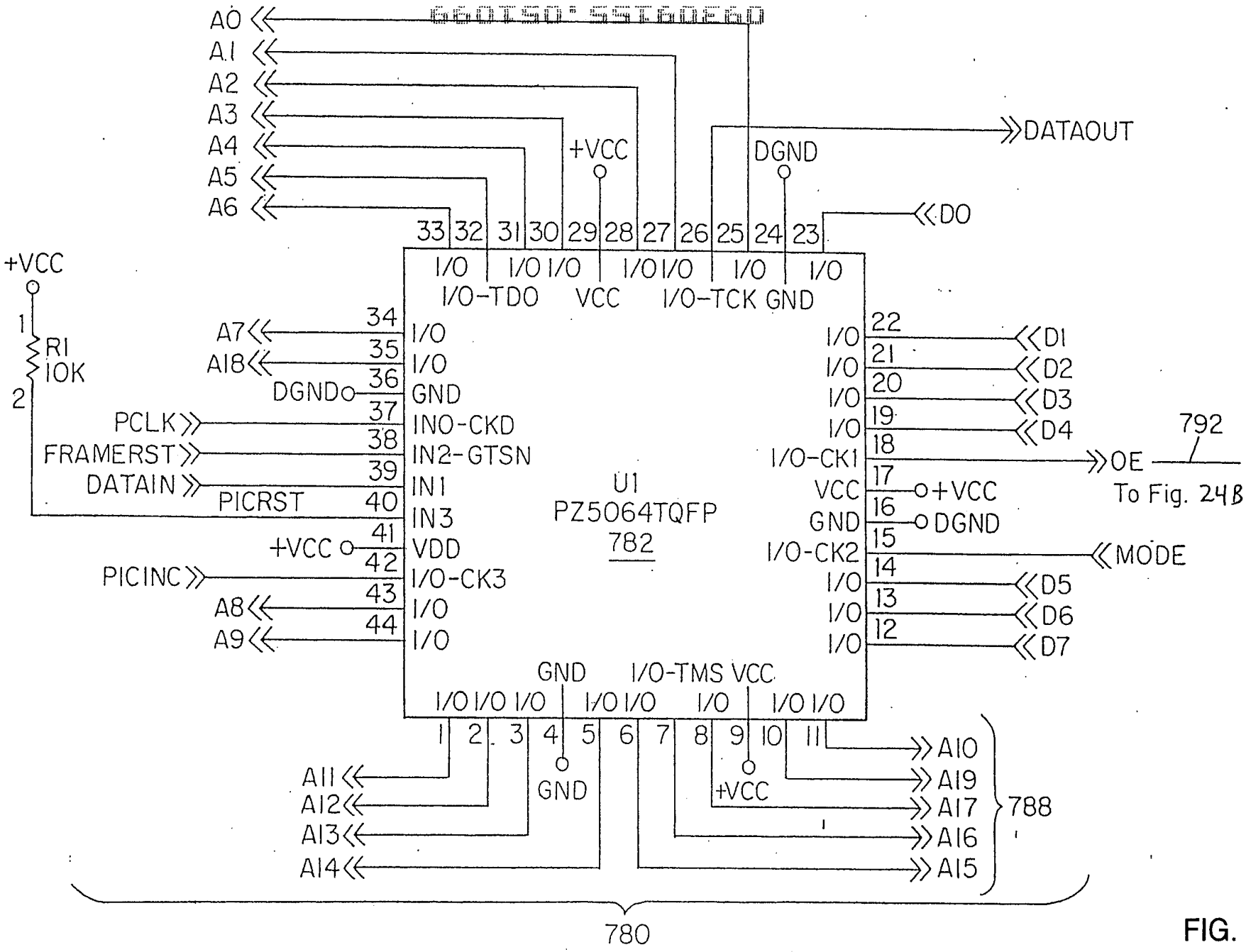

A0
A1
A2
A3
A4
A5
A6
DATAOUT
+VCC
DGND
DO
33 32 31 30 29 28 27 26 25 24 23
I/O I/O I/O I/O I/O I/O I/O I/O
I/O-TDO VCC I/O-TCK GND
+VCC
1
RI
10K
2
A7
A18
DGND
PCLK
FRAMERST
DATAIN
PICRST
34 I/O
35 I/O
36 GND
37 IN0-CKD
38 IN2-GTSN
39 IN1
40 IN3
41 VDD
42 I/O-CK3
43 I/O
44 I/O
+VCC
PICINC
A8
A9
U1
PZ5064TQFP
782
22 I/O
21 I/O
20 I/O
19 I/O
18 I/O-CK1
17 VCC
16 GND
15 I/O-CK2
14 I/O
13 I/O
12 I/O
D1
D2
D3
D4
OE
+VCC
DGND
MODE
D5
D6
D7
792
To Fig. 24B
GND I/O-TMS VCC
I/O I/O I/O I/O I/O I/O I/O I/O I/O
1 2 3 4 5 6 7 8 9 10 11
A11
A12
A13
A14
GND
+VCC
A10
A19
A17
A16
A15
788
780

FIG. 24A

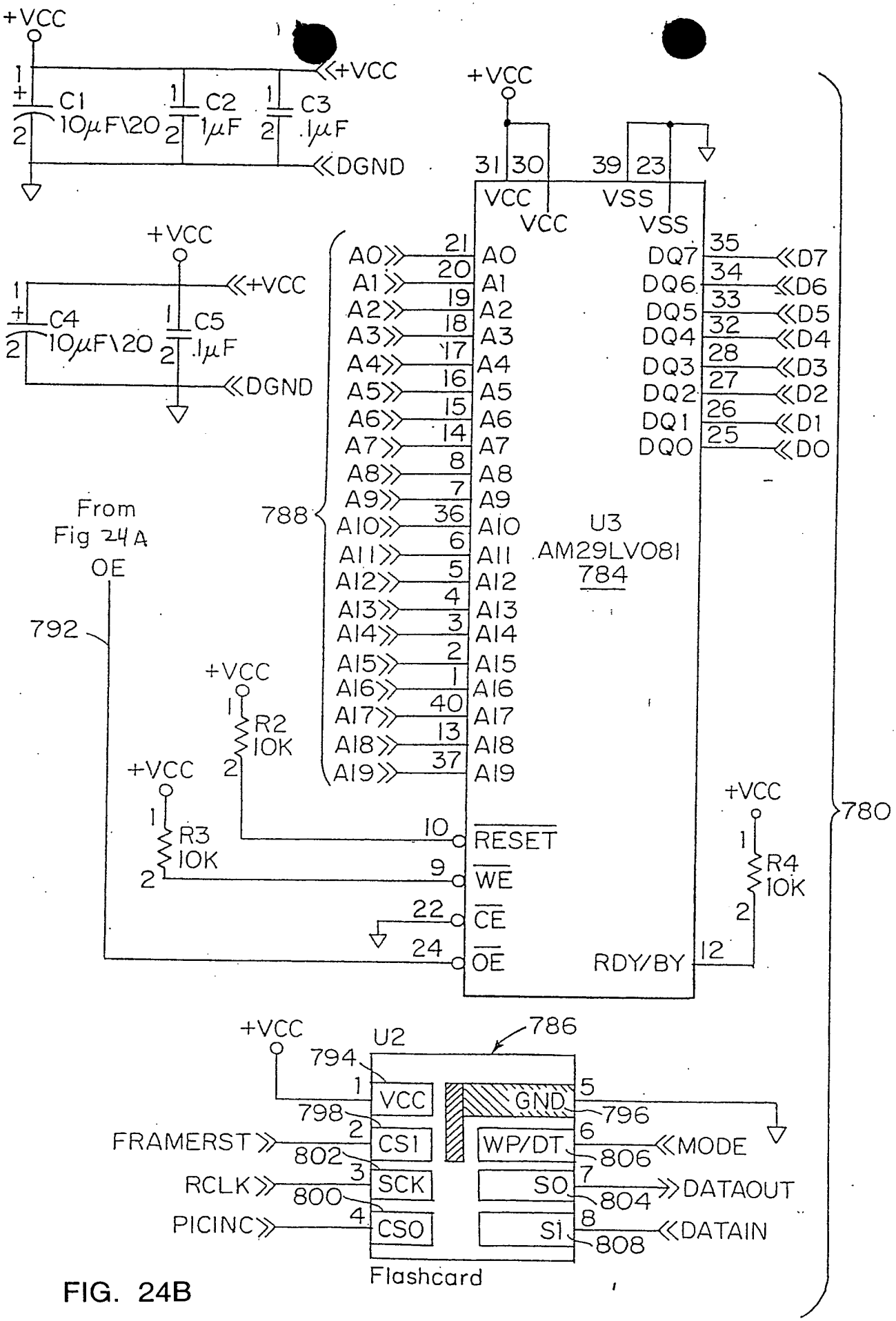

+VCC
C1
10μF\20
C2
1μF
C3
.1μF
DGND
C4
10μF\20
C5
.1μF
From
Fig 24A
OE
792
788
U3
AM29LV081
784
780
R2
10K
R3
10K
R4
10K
RESET
WE
CE
OE
RDY/BY
VCC
VSS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
D7
D6
D5
D4
D3
D2
D1
D0
U2
786
794
798
802
800
796
806
804
808
VCC
CS1
SCK
CSO
GND
WP/DT
SO
SI
FRAMERST
RCLK
PICINC
MODE
DATAOUT
DATAIN
Flashcard

FIG. 24B

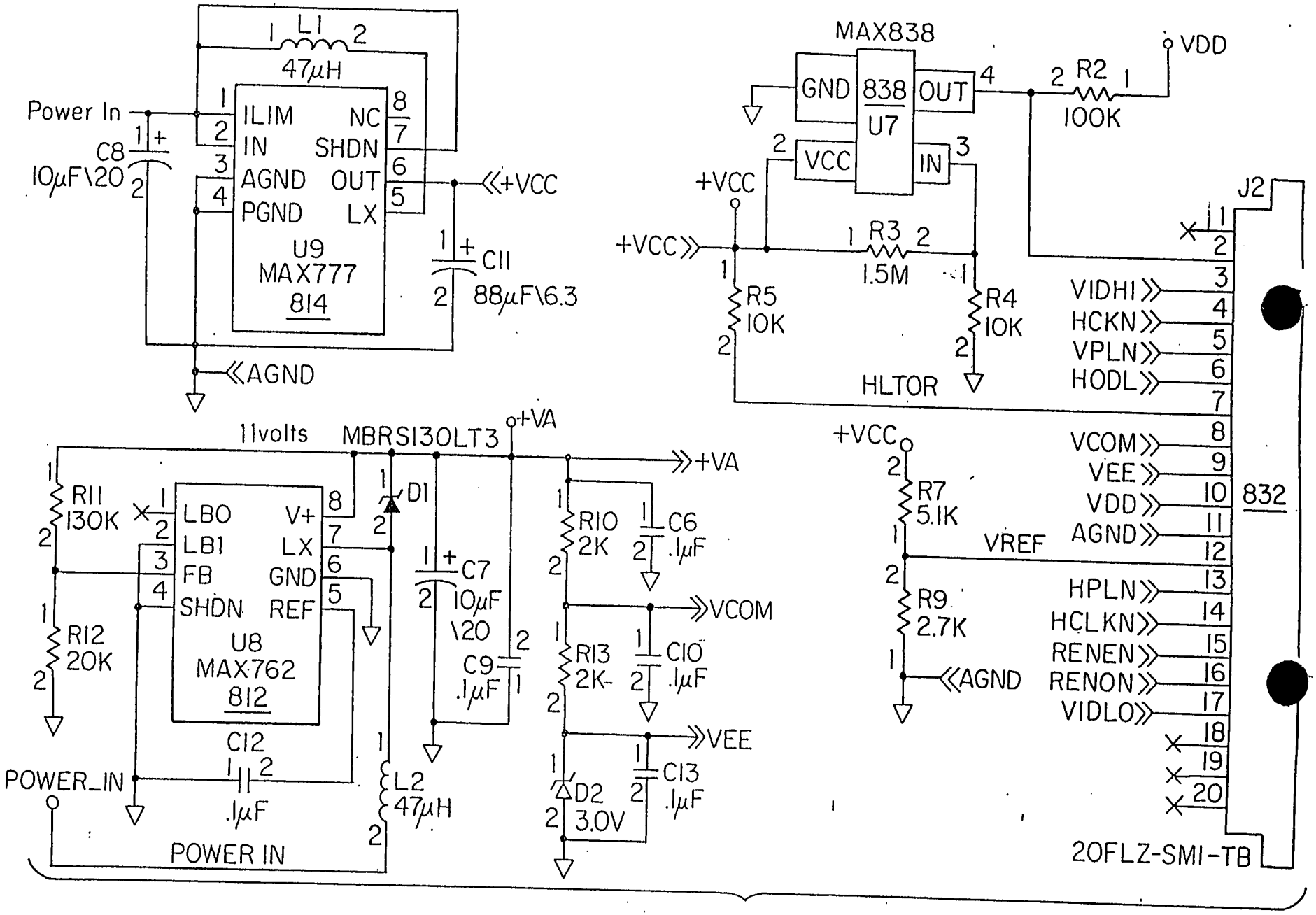

L1
47µH
Power In
C8
10µF\20
U9
MAX777
814
ILIM
IN
AGND
PGND
NC
SHDN
OUT
LX
+VCC
C11
88µF\6.3
AGND
MAX838
GND
838
U7
OUT
VCC
IN
VDD
R2
100K
R3
1.5M
R4
10K
R5
10K
HLTOR
J2
VIDHI
HCKN
VPLN
HODL
VCOM
VEE
VDD
AGND
VREF
R7
5.1K
R9
2.7K
HPLN
HCLKN
RENEN
RENON
VIDLO
832
20FLZ-SMI-TB
11volts
MBRS130LT3
+VA
R11
130K
R12
20K
U8
MAX762
812
LBO
LB1
FB
SHDN
V+
LX
GND
REF
D1
C7
10µF
\20
C9
.1µF
C12
.1µF
L2
47µH
POWER_IN
POWER IN
R10
2K
C6
.1µF
R13
2K-
C10
.1µF
D2
3.0V
C13
.1µF

FIG. 25A

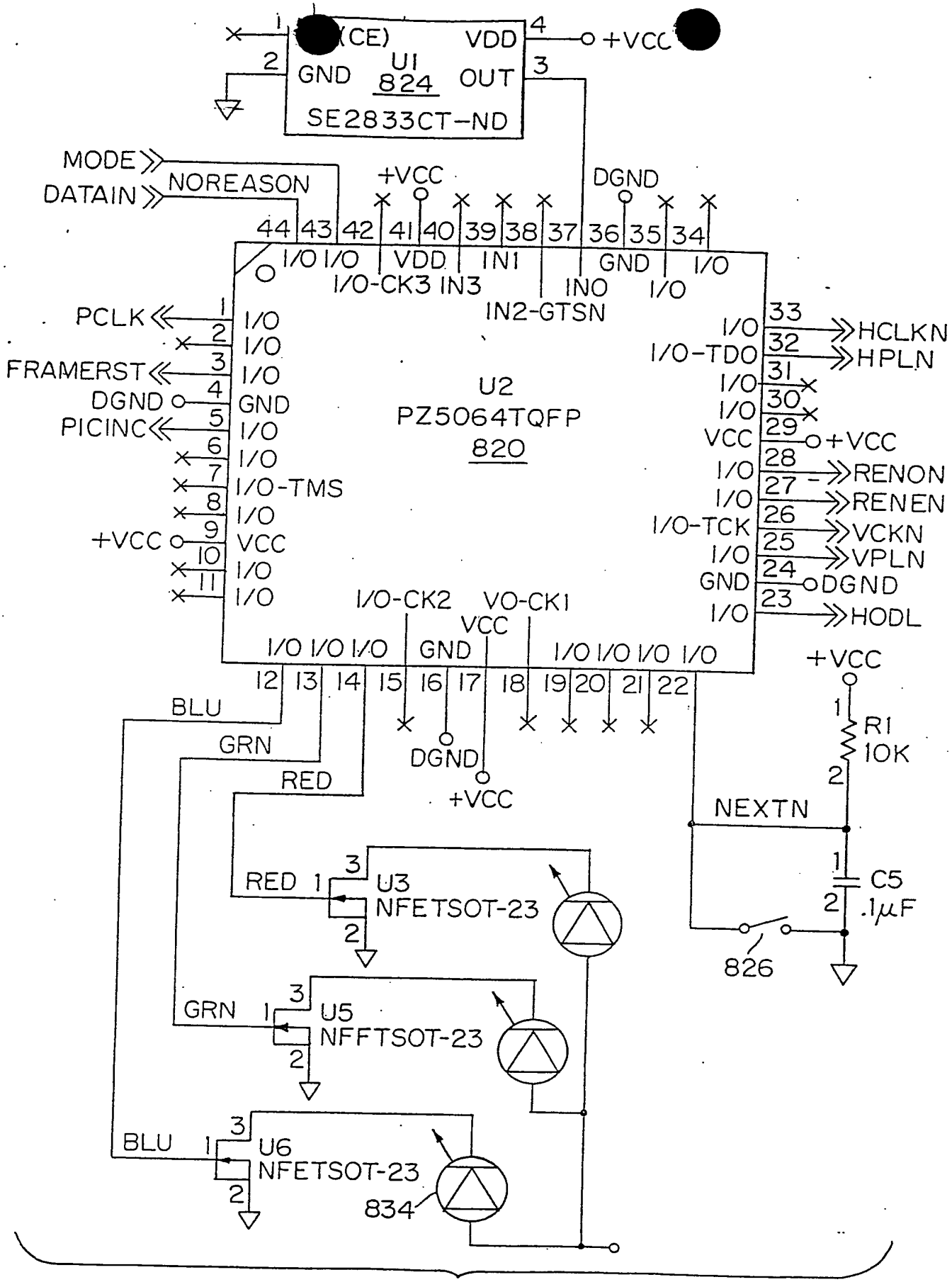

U1
824
SE2833CT-ND
(CE)
VDD
GND
OUT
+VCC
MODE
DATAIN
NOREASON
DGND
U2
PZ5064TQFP
820
PCLK
FRAMERST
PICINC
I/O-TMS
HCLKN
HPLN
RENON
RENEN
VCKN
VPLN
HODL
I/O-TDO
I/O-TCK
I/O-CK3 IN3
IN2-GTSN
I/O-CK2
VO-CK1
BLU
GRN
RED
R1
10K
NEXTN
C5
.1μF
826
U3
NFETSOT-23
U5
NFFTSOT-23
U6
NFETSOT-23
834

FIG. 25B

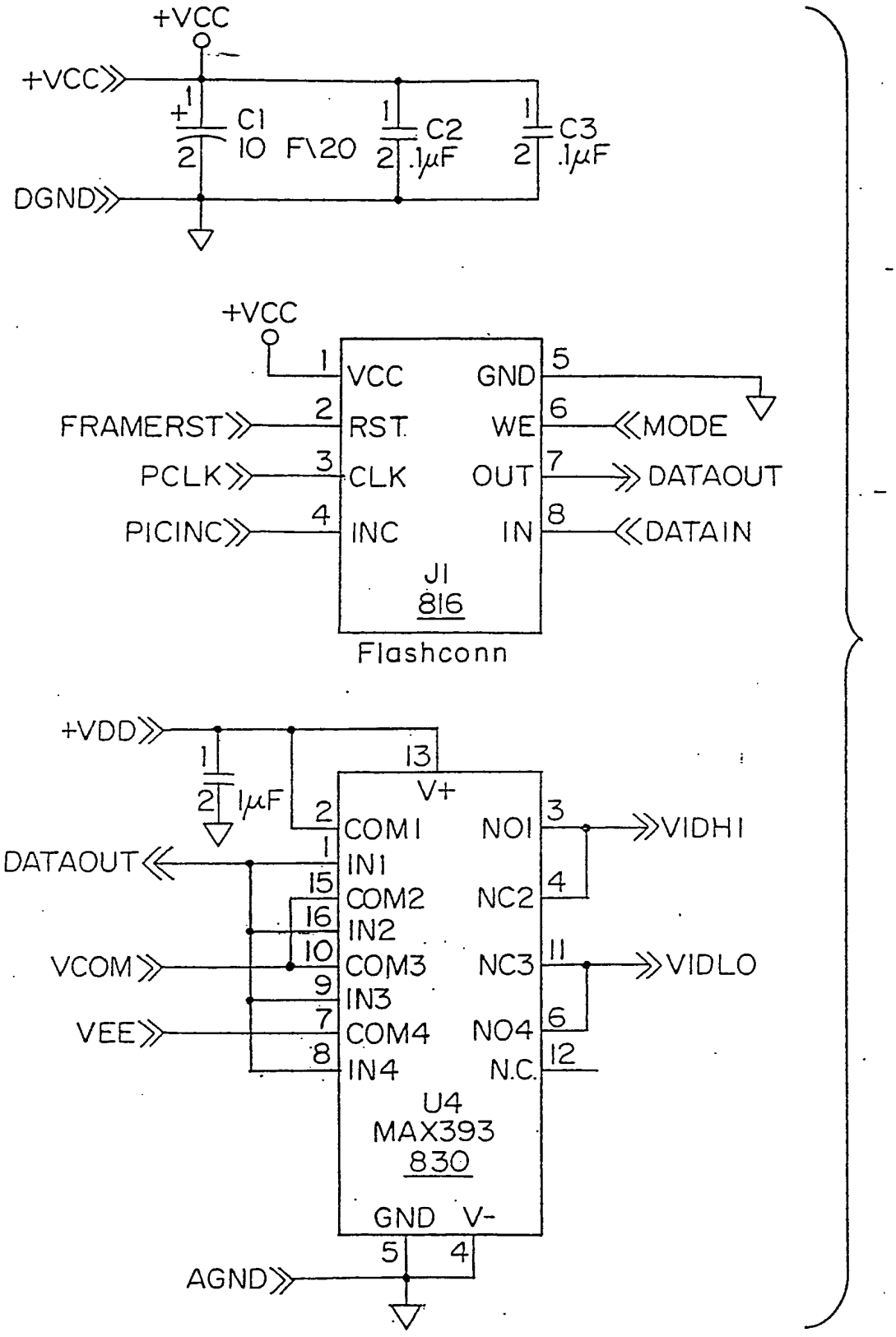

+VCC
+VCC
C1
10 F\20
C2
.1μF
C3
.1μF
DGND
+VCC
VCC
GND
FRAMERST
RST
WE
MODE
PCLK
CLK
OUT
DATAOUT
PICINC
INC
IN
DATAIN
J1
816
Flashconn
+VDD
1μF
V+
COM1
NO1
VIDHI
DATAOUT
IN1
COM2
NC2
IN2
VCOM
COM3
NC3
VIDLO
IN3
VEE
COM4
NO4
IN4
N.C.
U4
MAX393
830
GND
V-
AGND

FIG. 25C

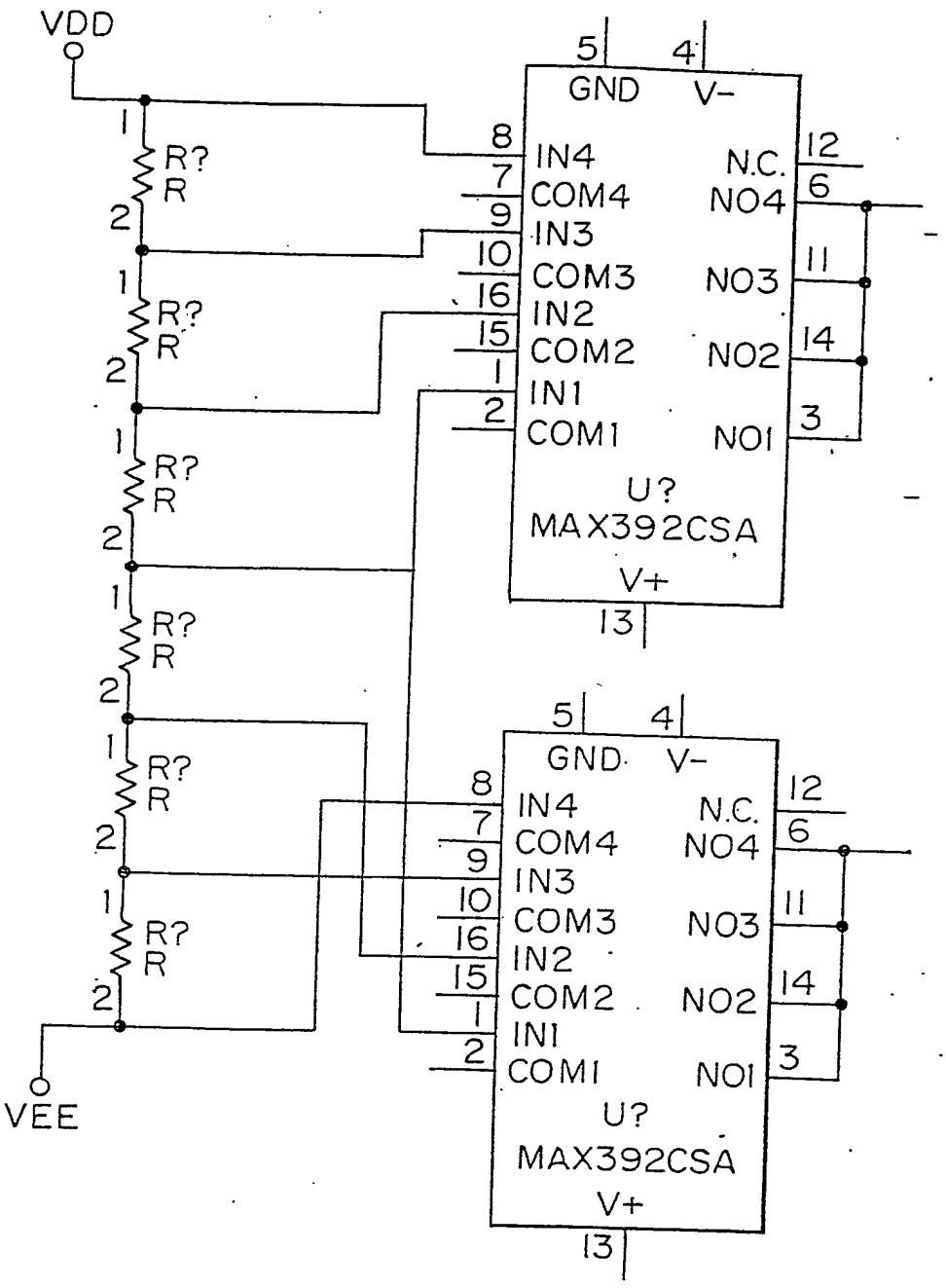

VDD
VEE
R?
R
U?
MAX392CSA
GND
V-
V+
IN4
COM4
IN3
COM3
IN2
COM2
IN1
COM1
N.C.
NO4
NO3
NO2
NO1

FIG. 26

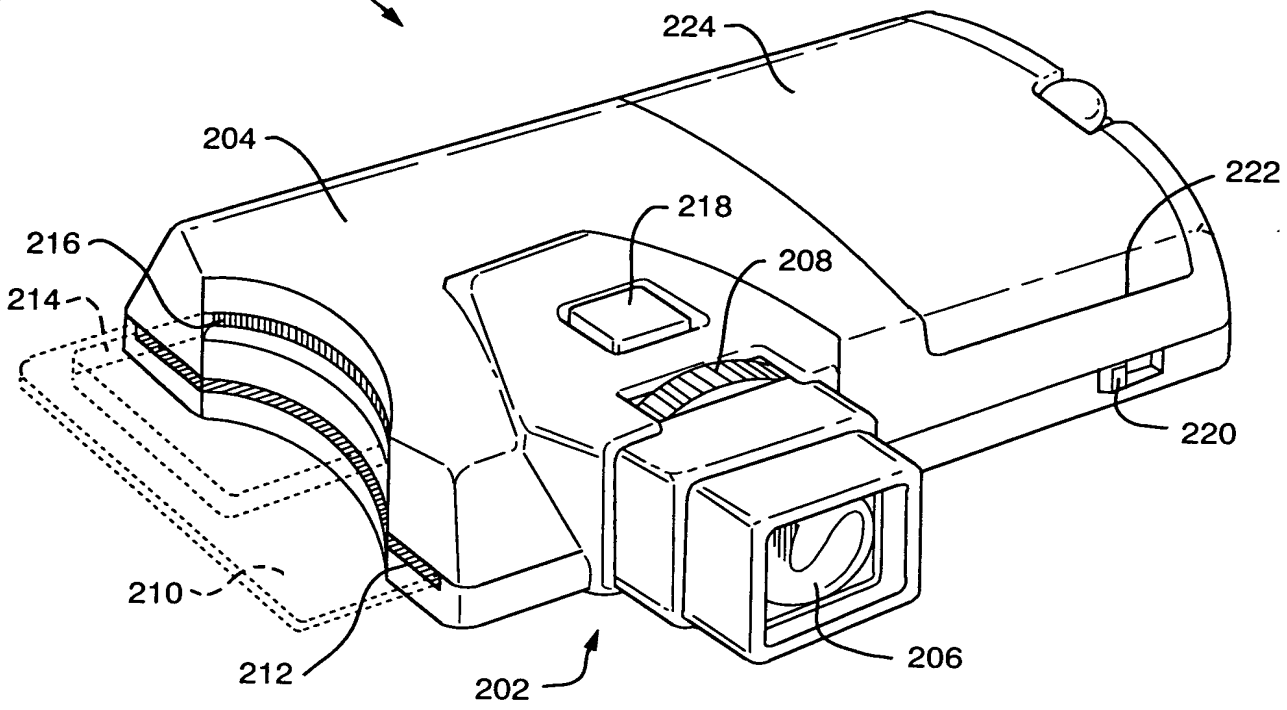


FIG. 27A

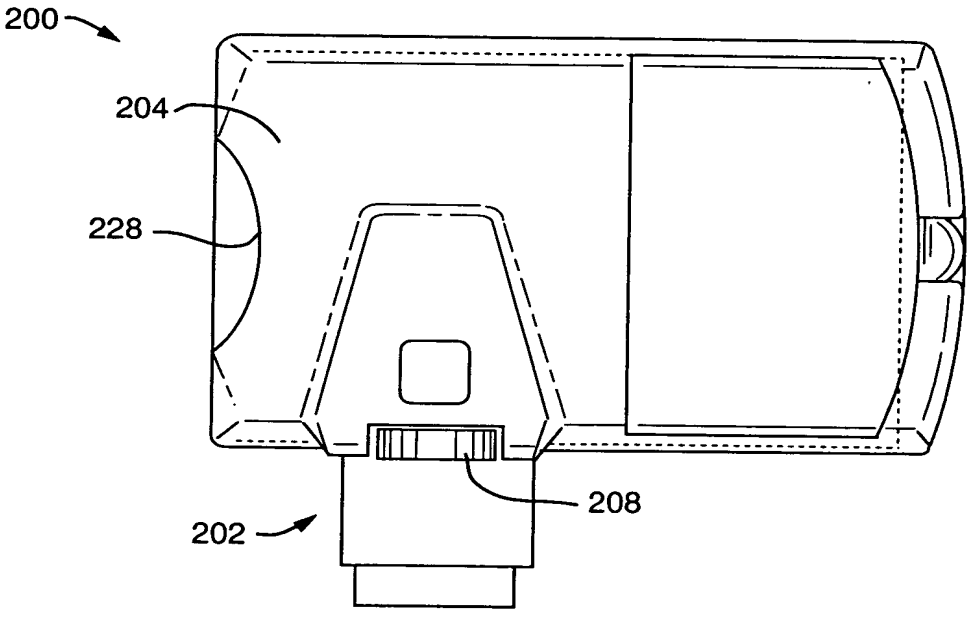


FIG. 27B

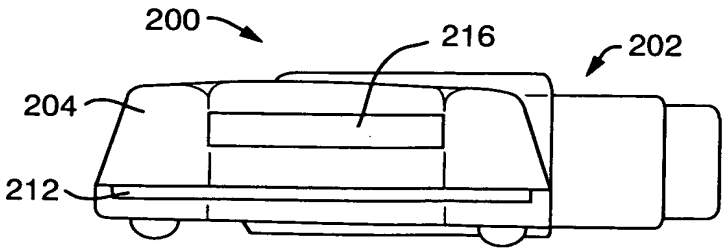


FIG. 27C

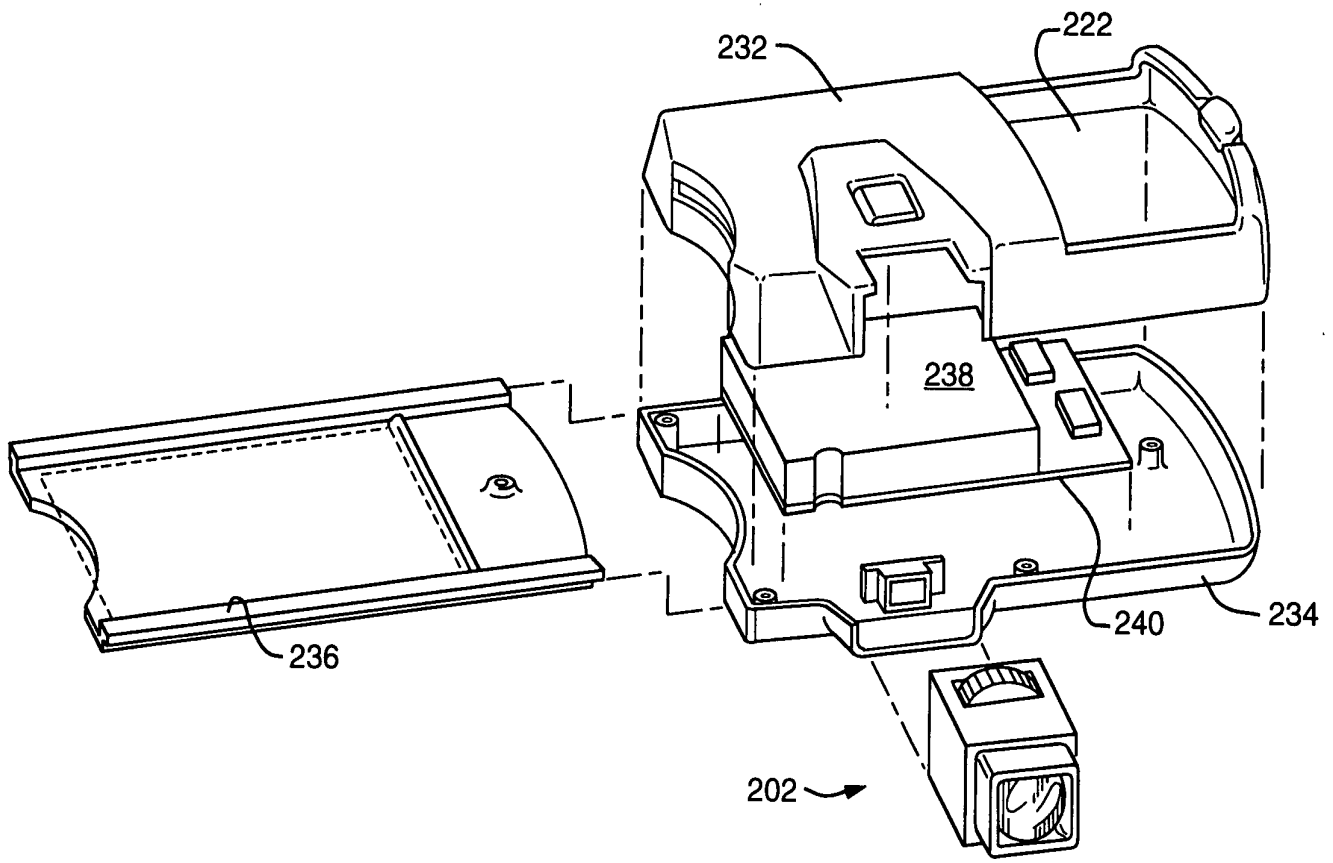


FIG. 27D

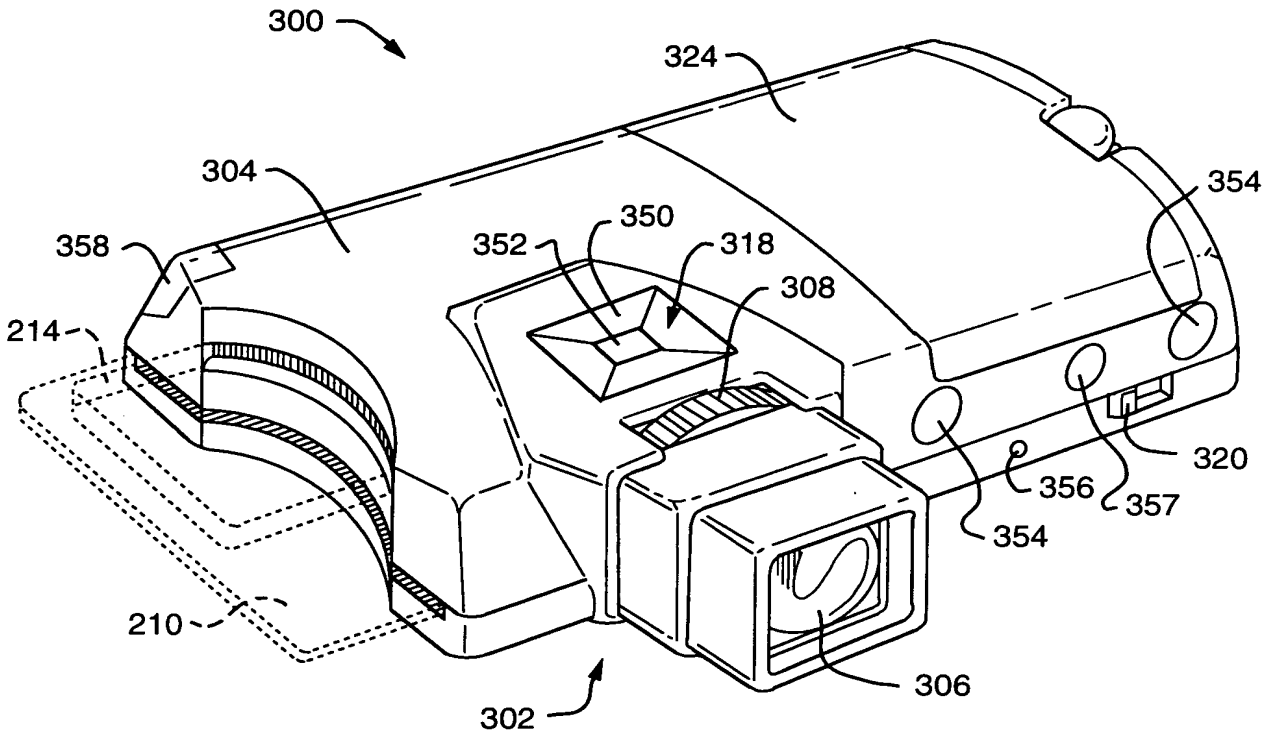


FIG. 28A

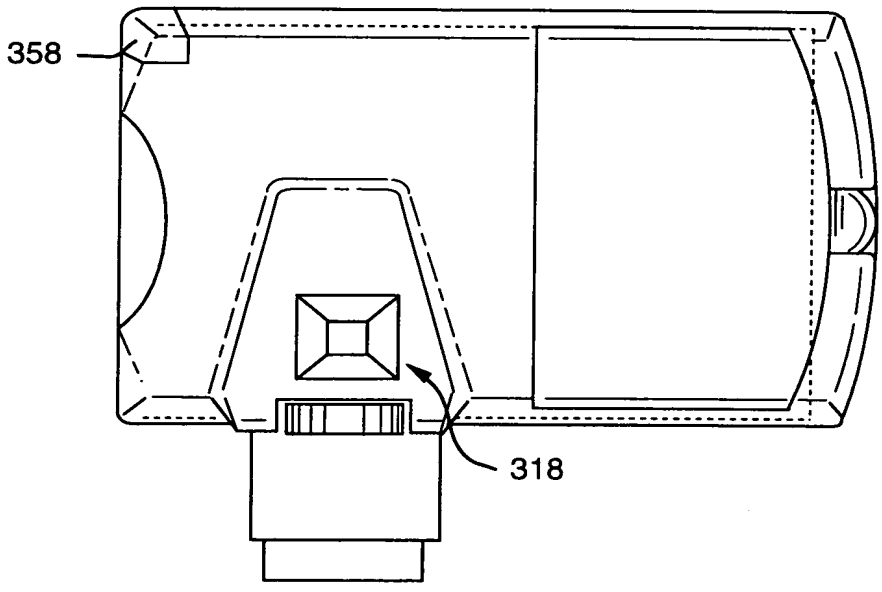


FIG. 28B

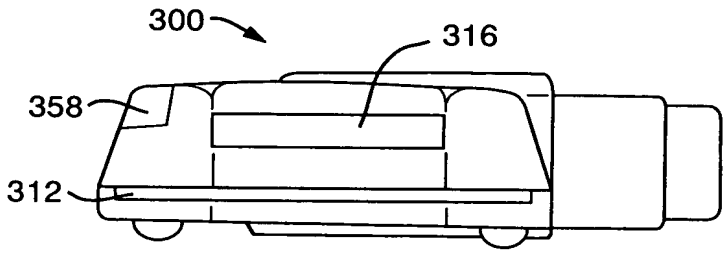


FIG. 28C

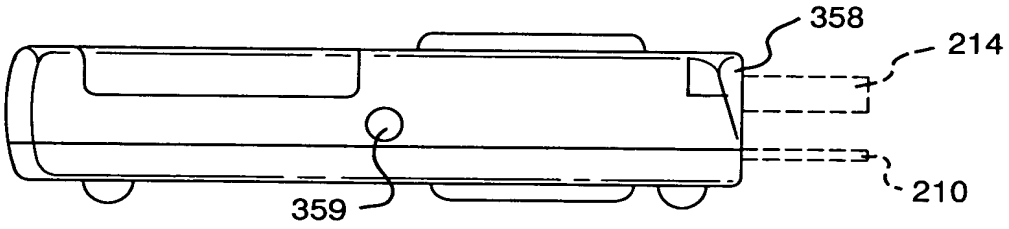


FIG. 28D

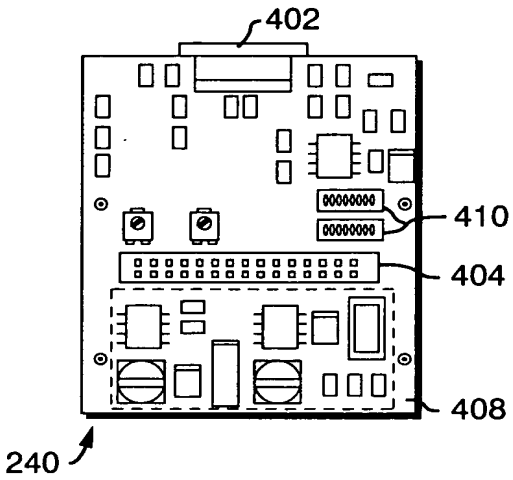


FIG. 29Aa

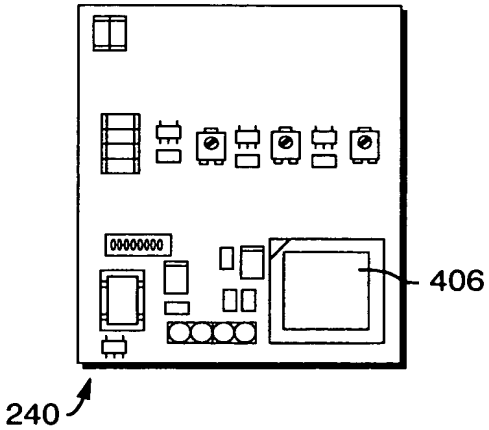


FIG. 29Ab

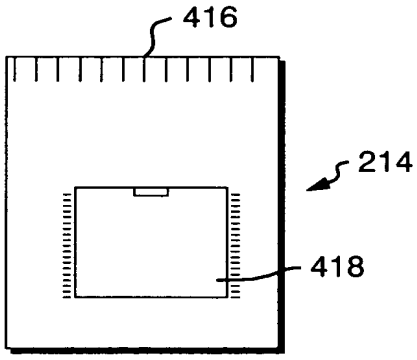


FIG. 29Ba

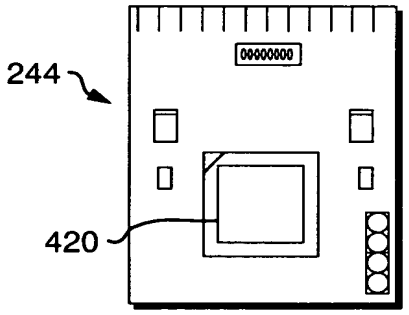


FIG. 29Bb

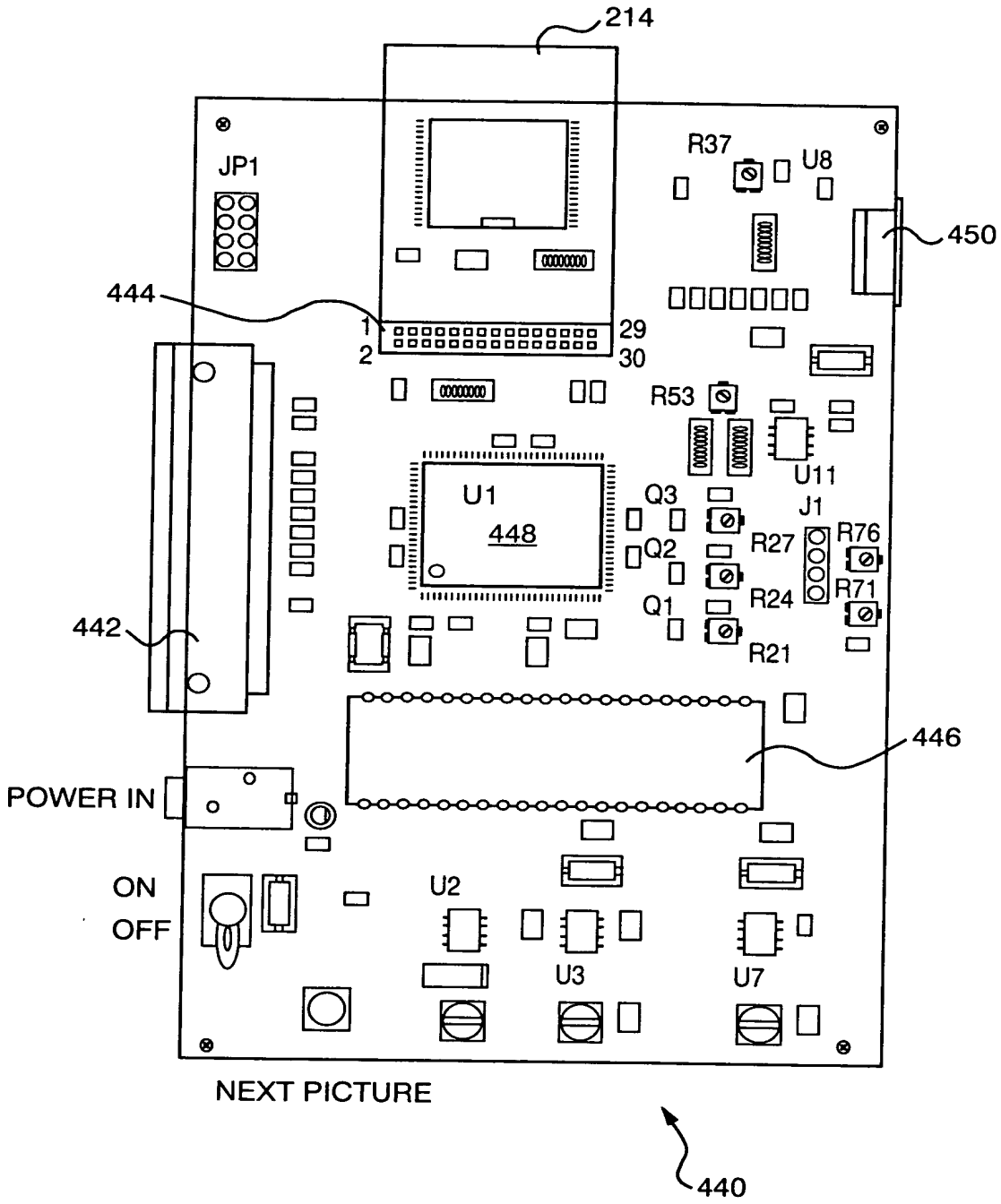

214
JP1
R37
U8
450
444
1
2
29
30
R53
U11
U1
448
Q3
J1
Q2
R27
R76
R24
R71
Q1
R21
442
446
POWER IN
ON
OFF
U2
U3
U7
NEXT PICTURE
440

FIG. 29C

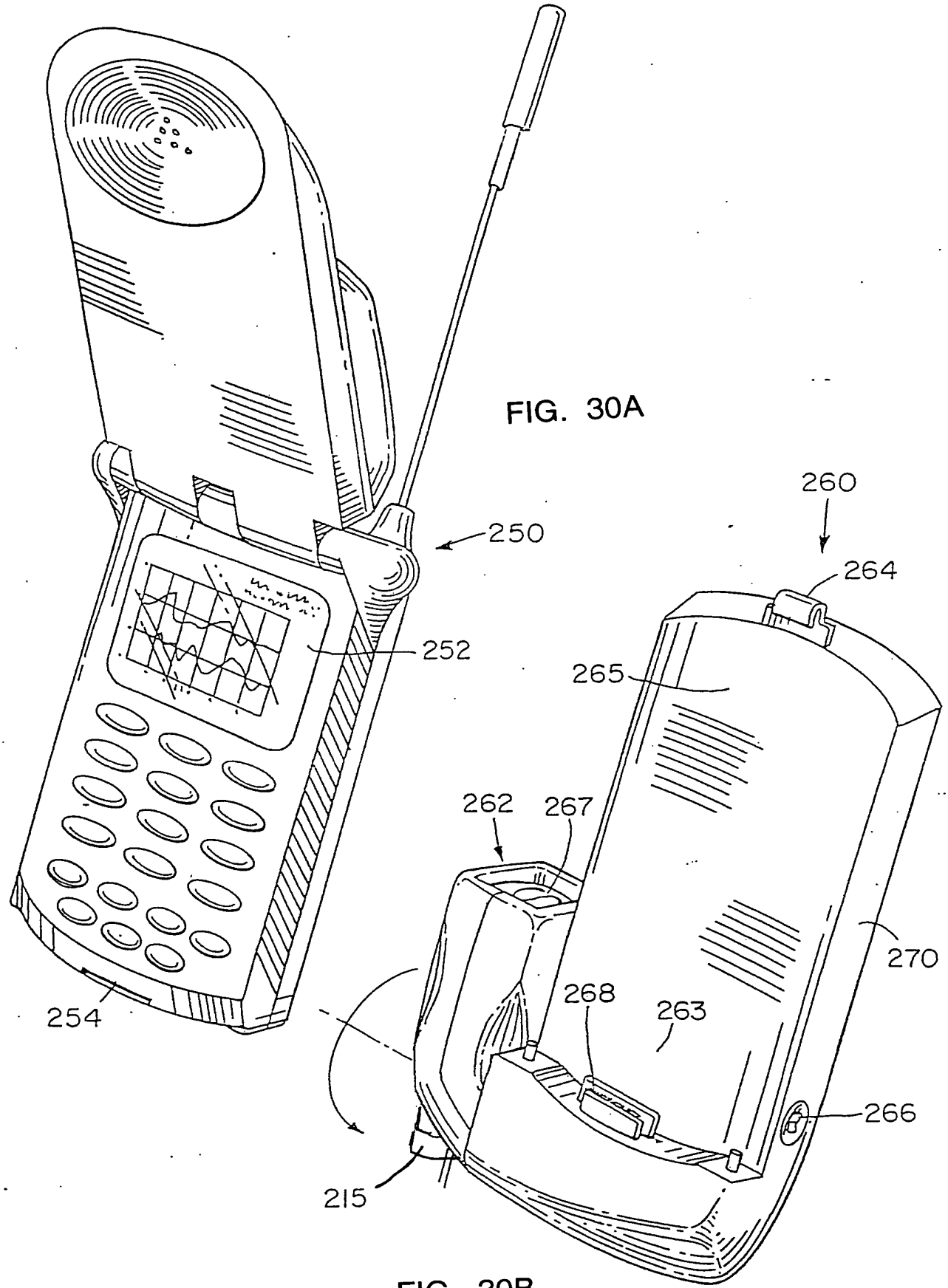


FIG. 30A

FIG. 30B

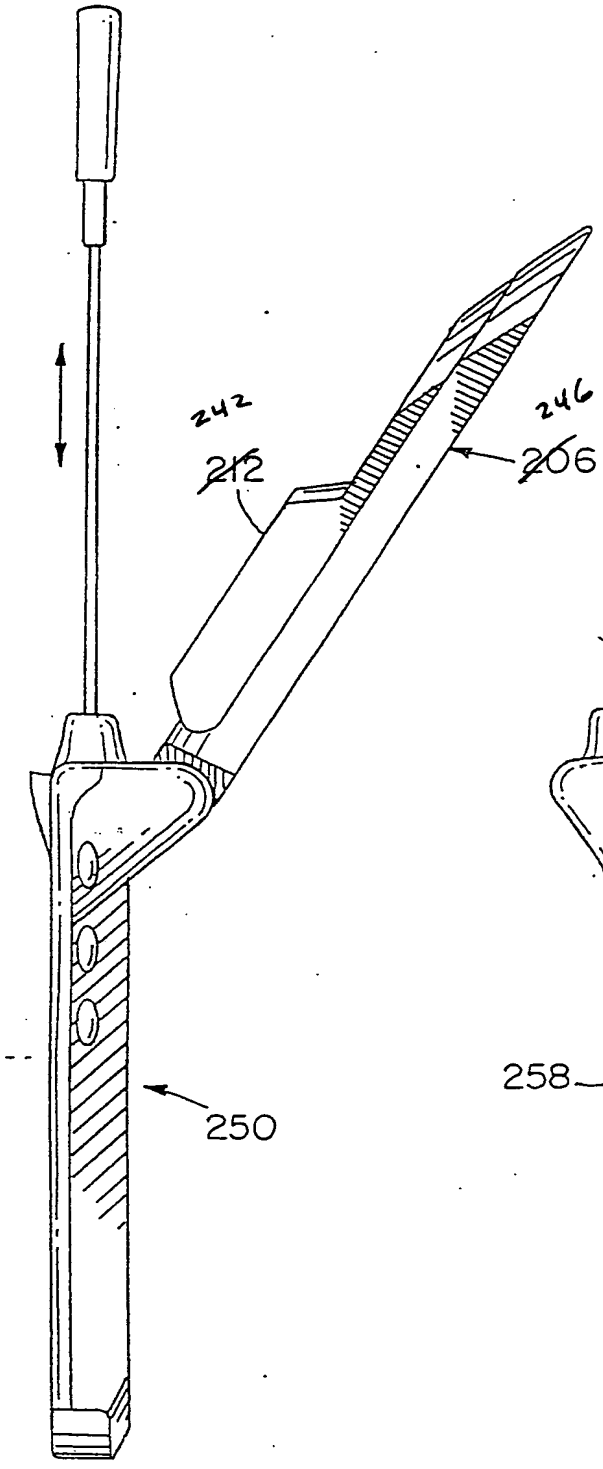


FIG. 30C

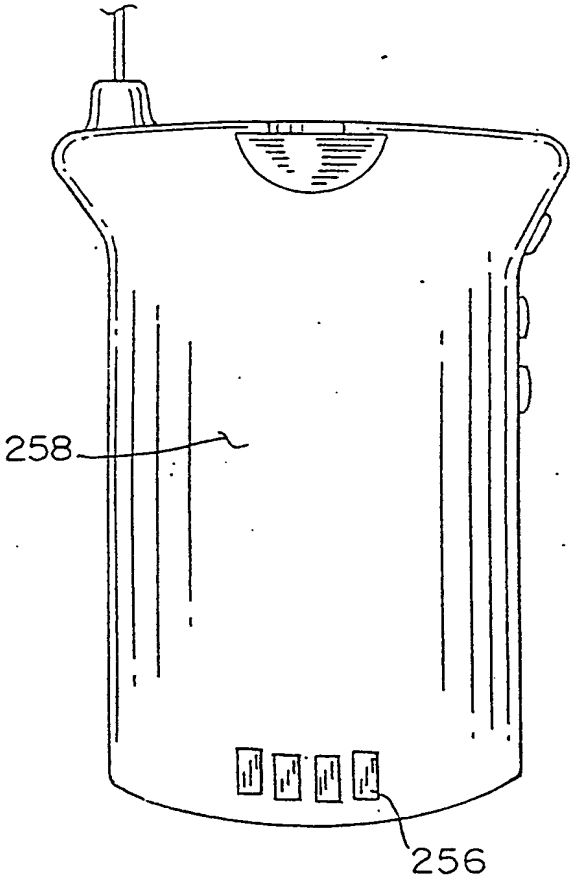


FIG. 30D

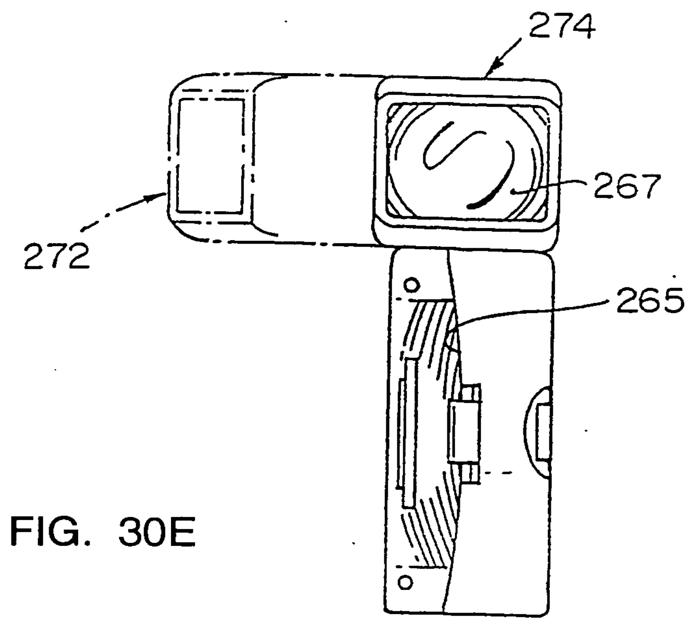


FIG. 30E

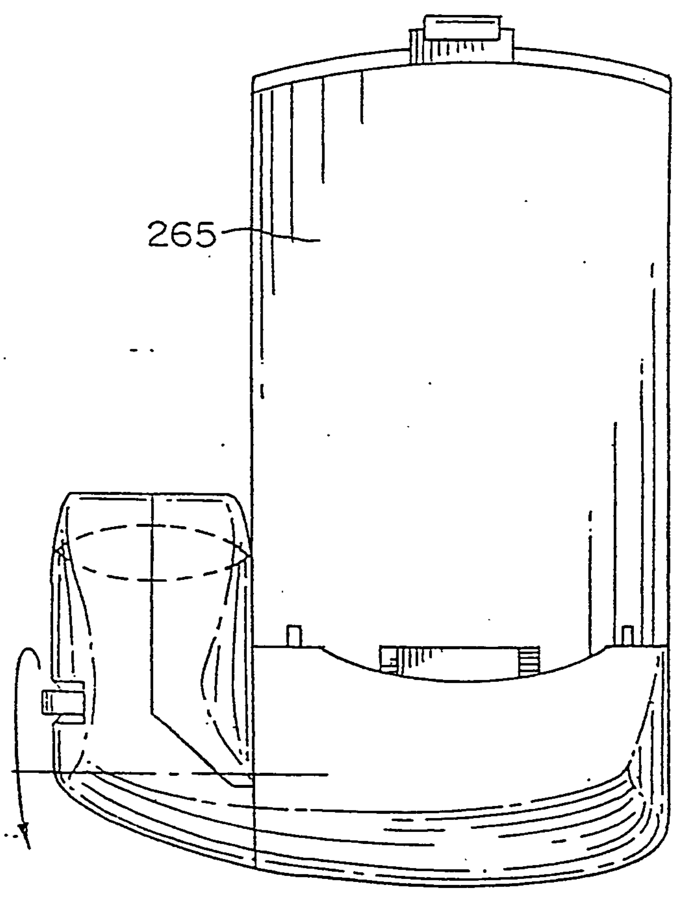


FIG. 30F

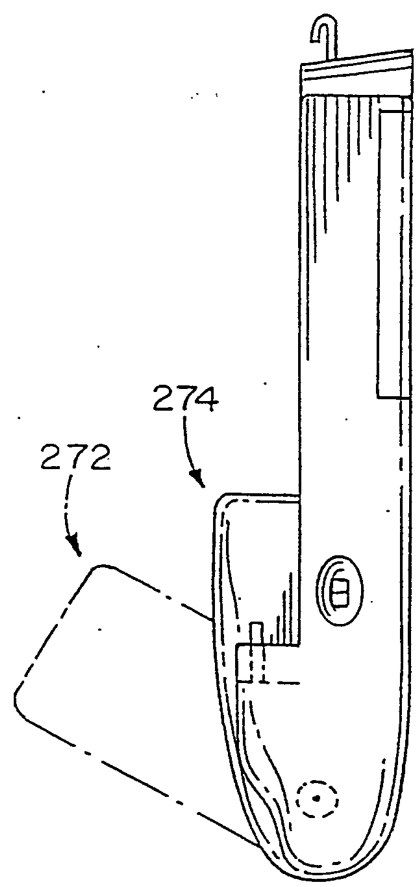


FIG. 30G

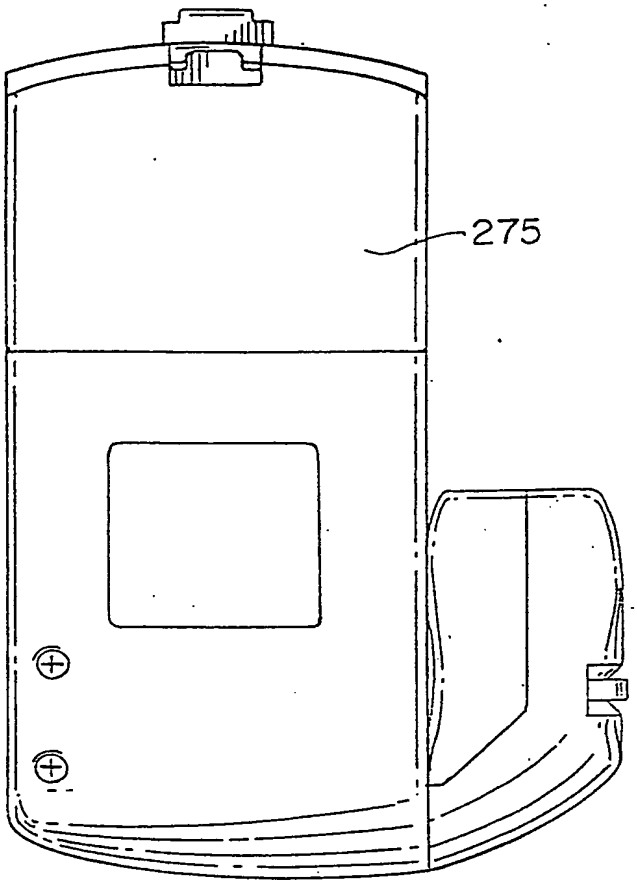


FIG. 30H

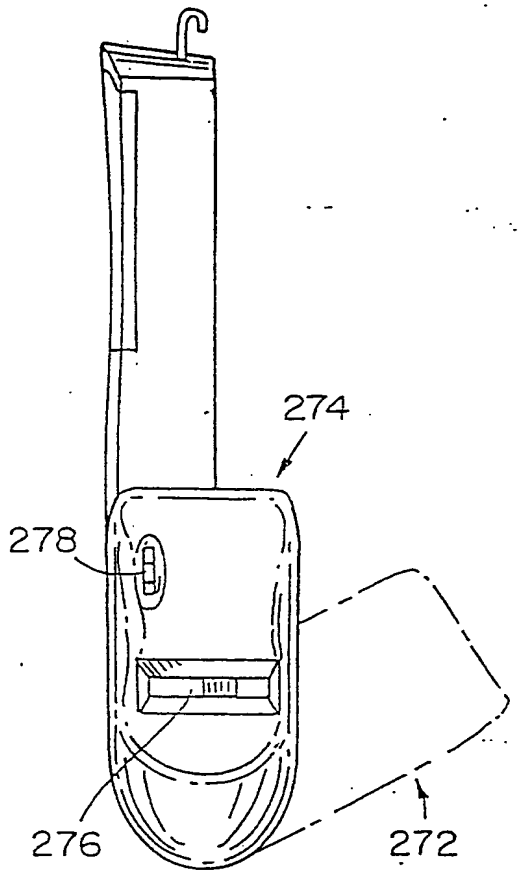


FIG. 30I

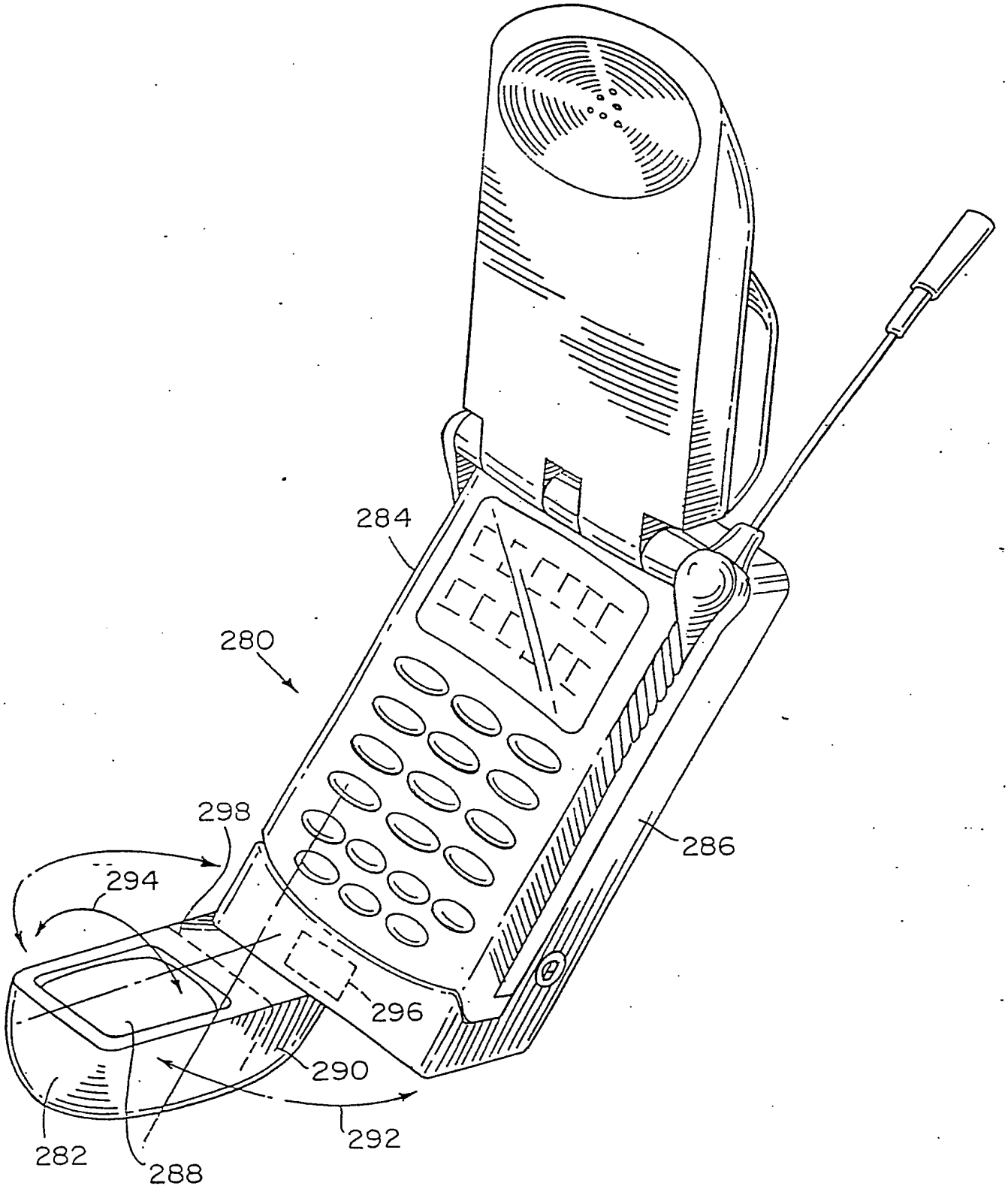


FIG. 30J

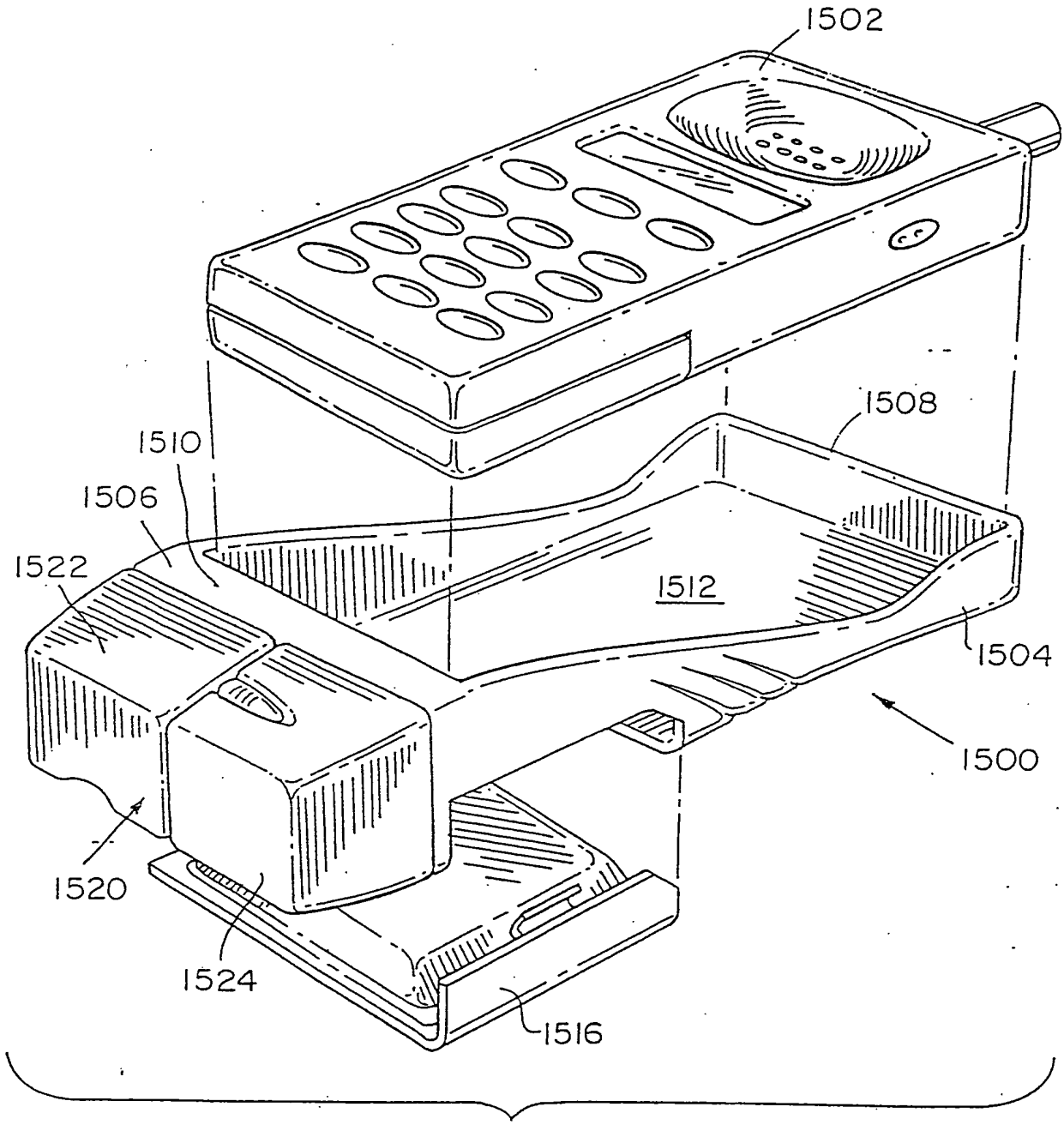


FIG. 31A

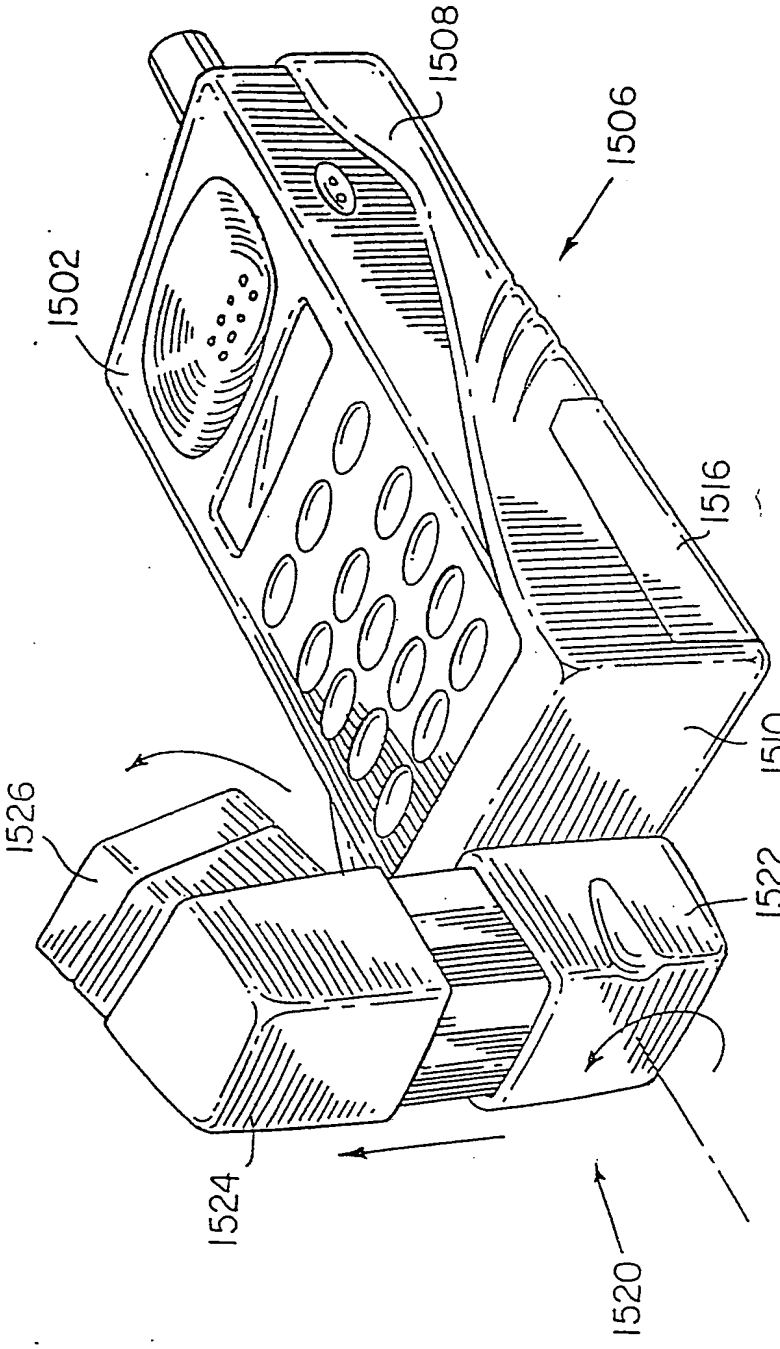


FIG. 31B

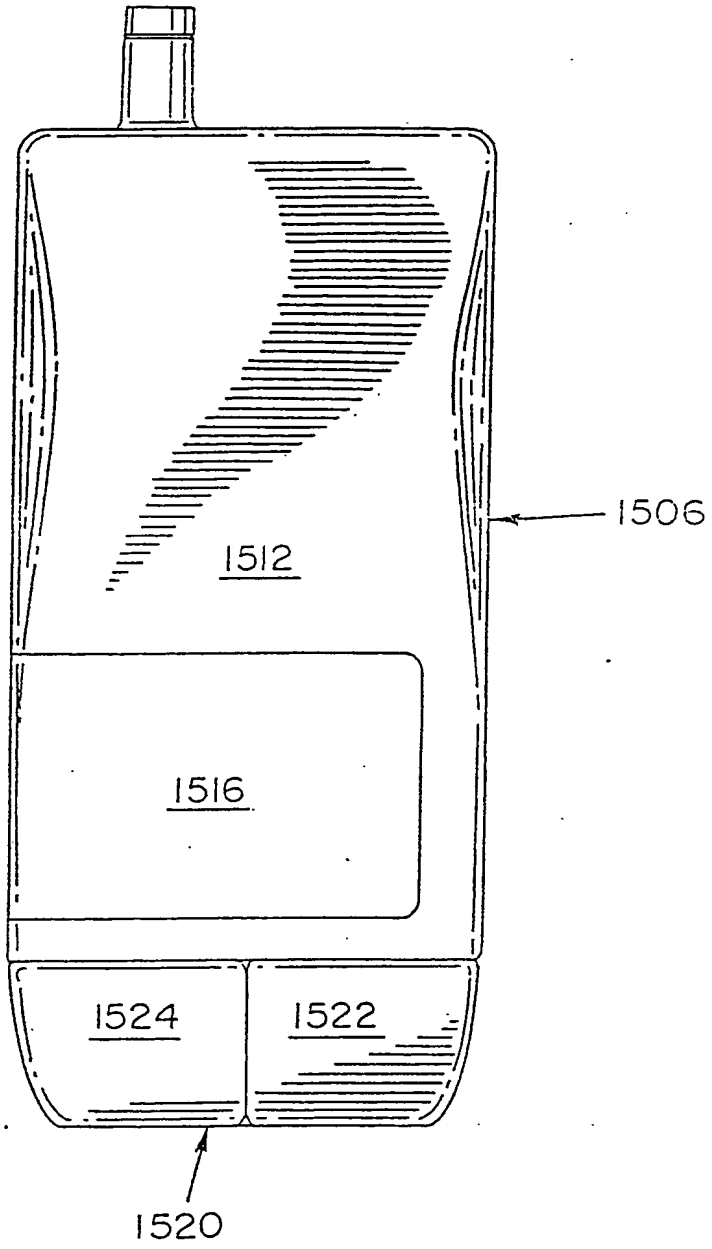


FIG. 31C

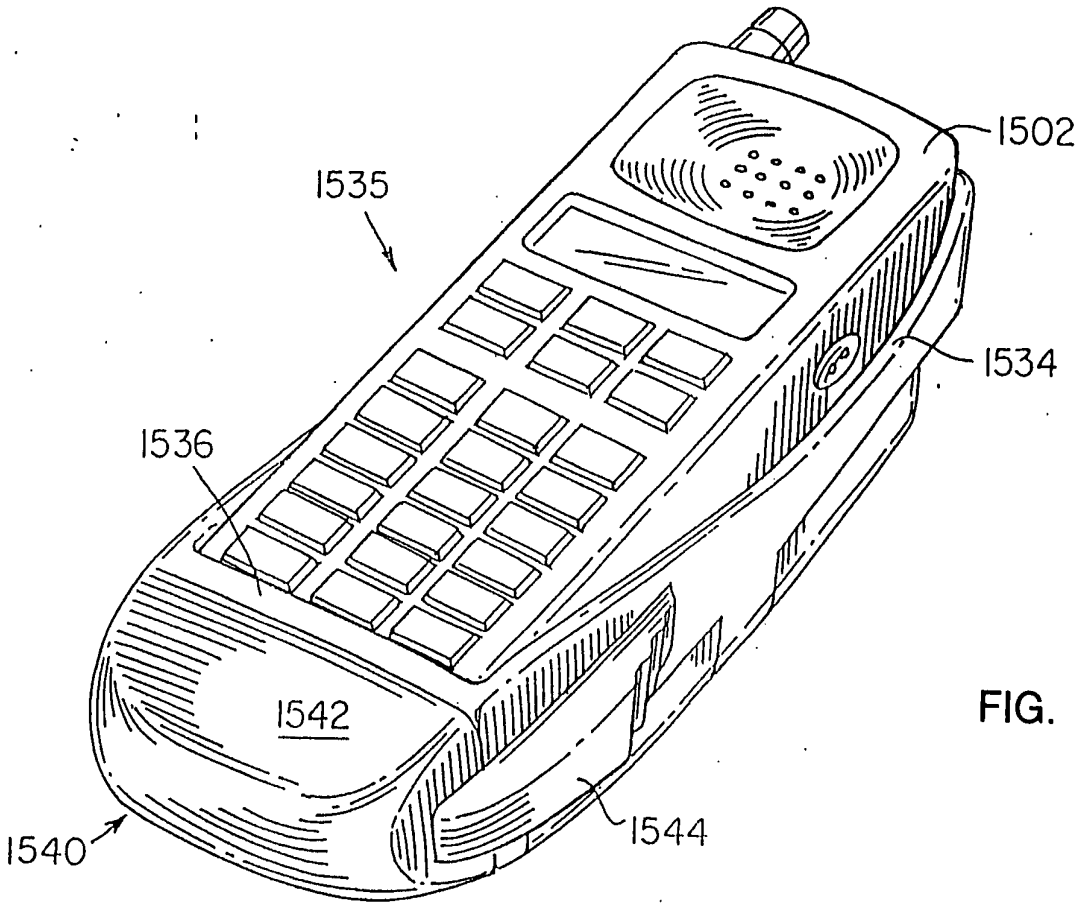


FIG. 31D

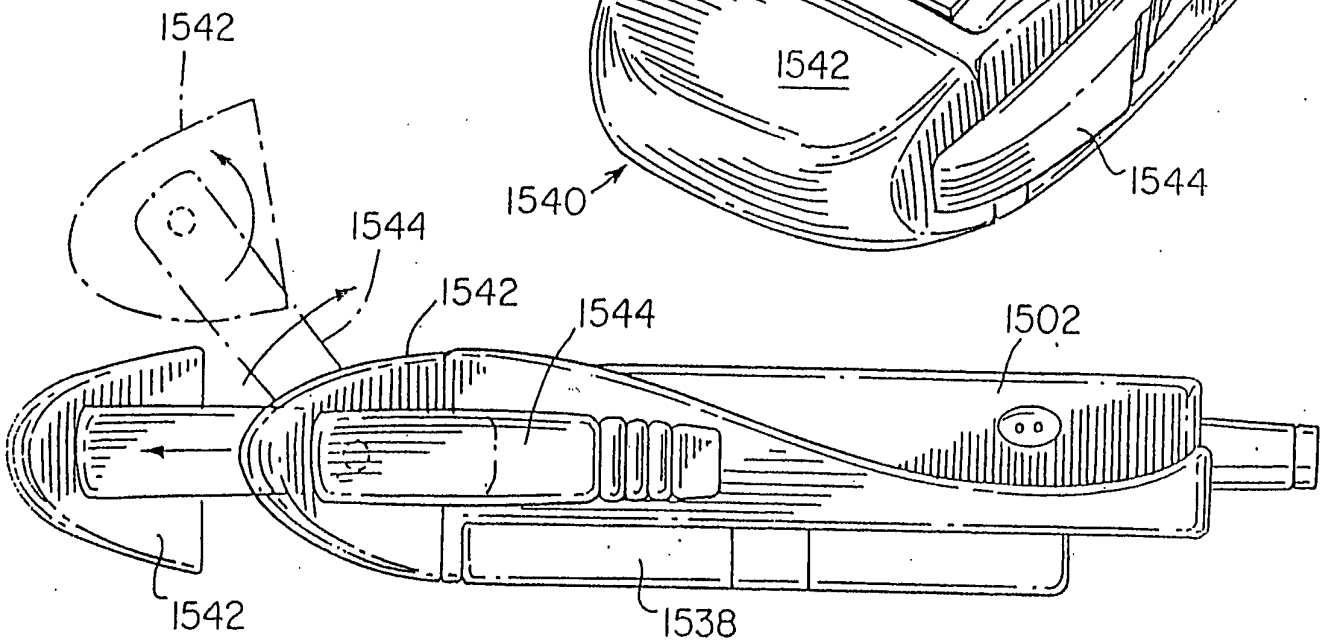


FIG. 31E

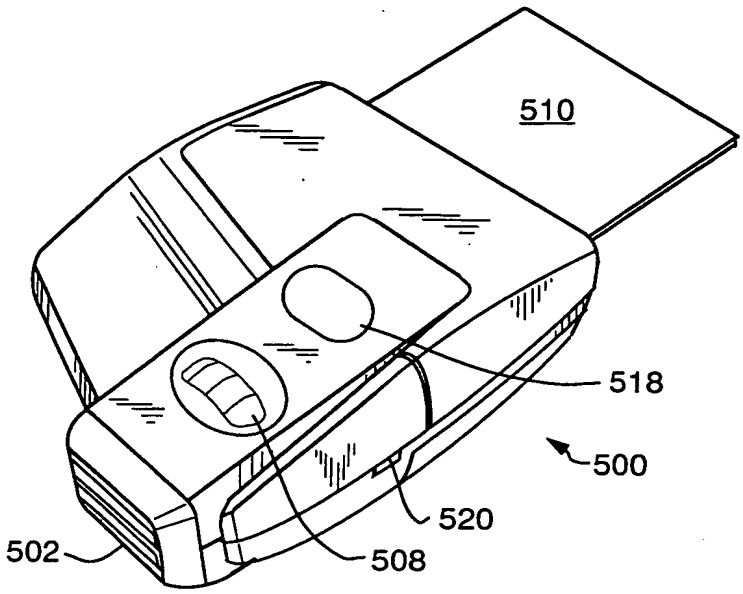


FIG. 32A

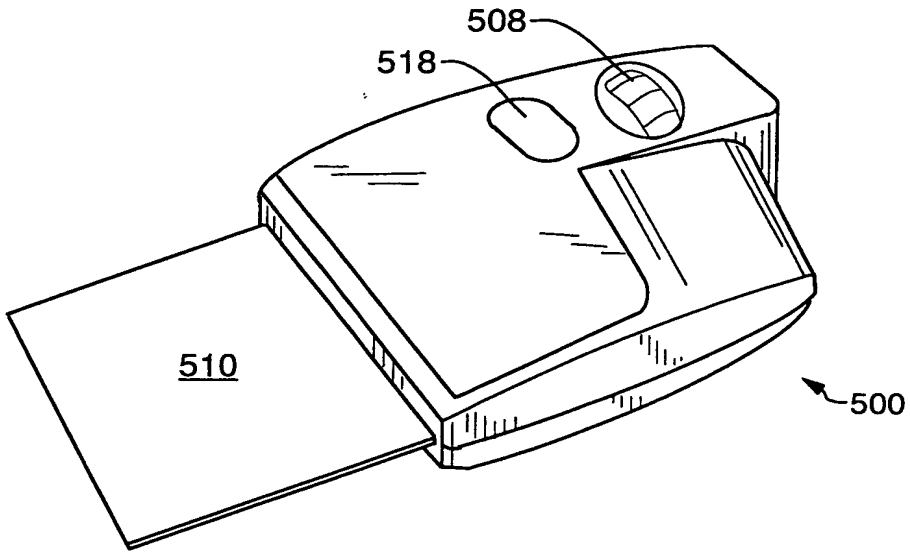


FIG. 32B

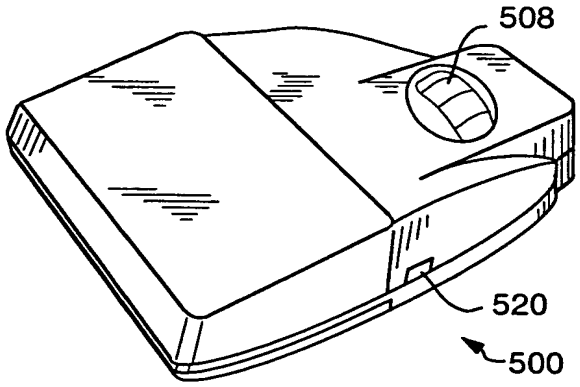


FIG. 32C

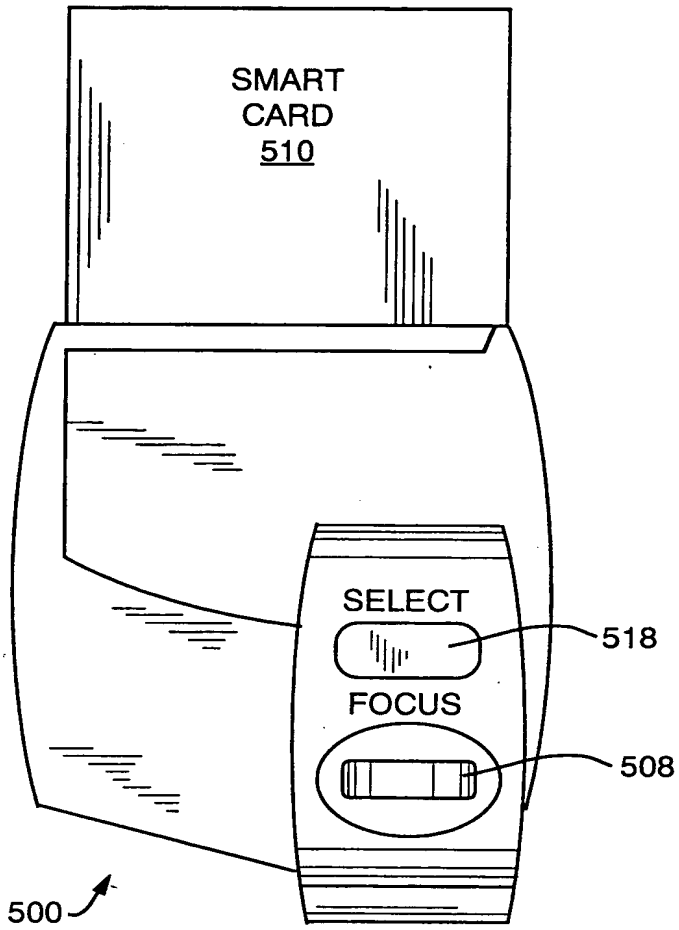


FIG. 32D

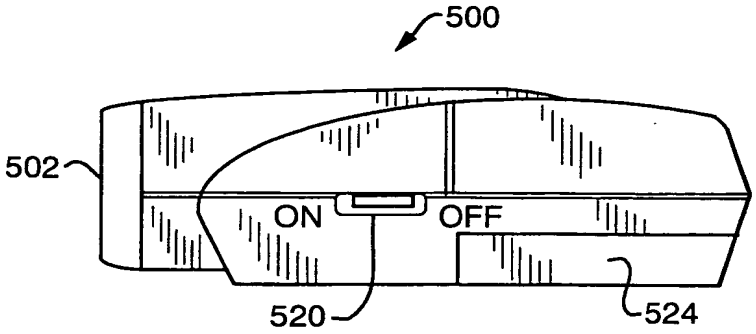


FIG. 32E

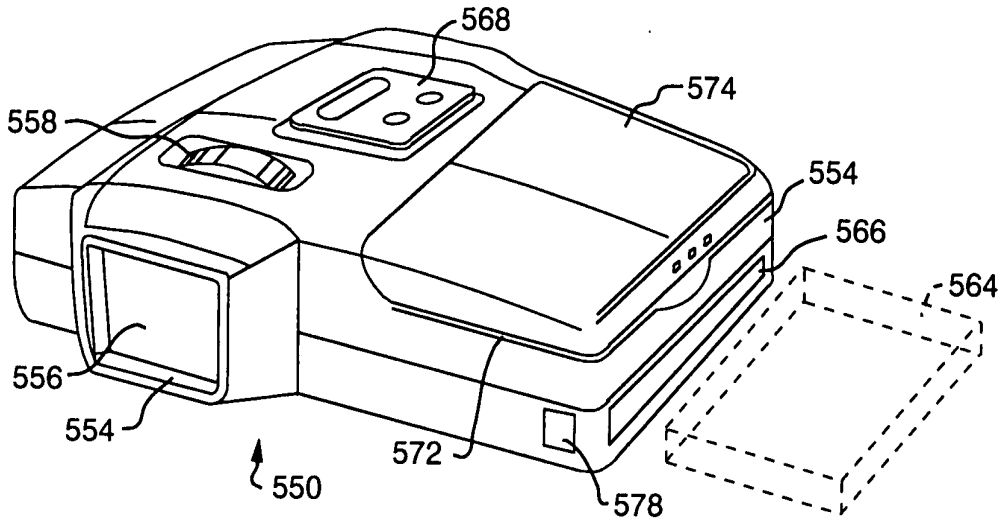


FIG. 33A

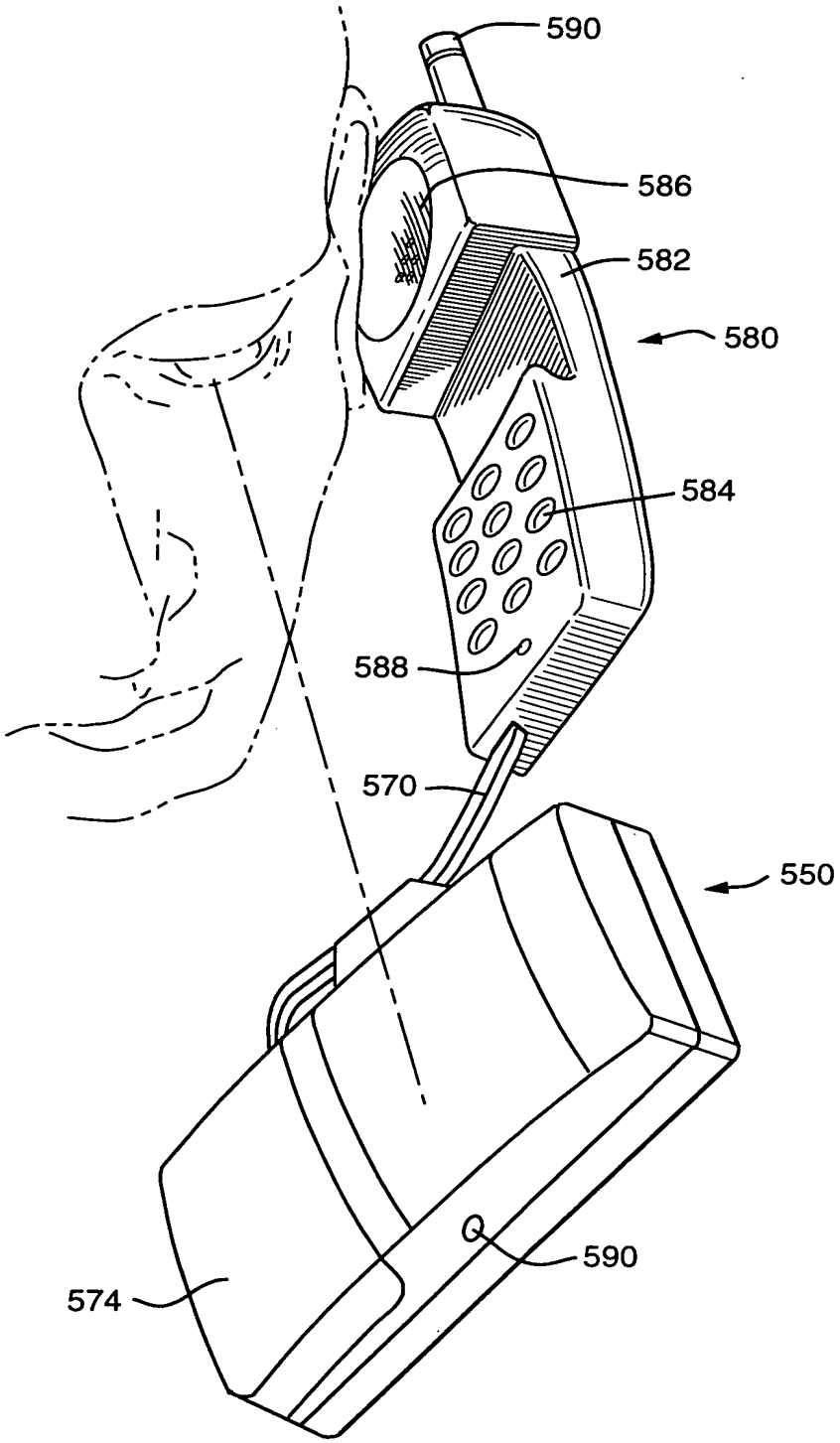


FIG. 33B

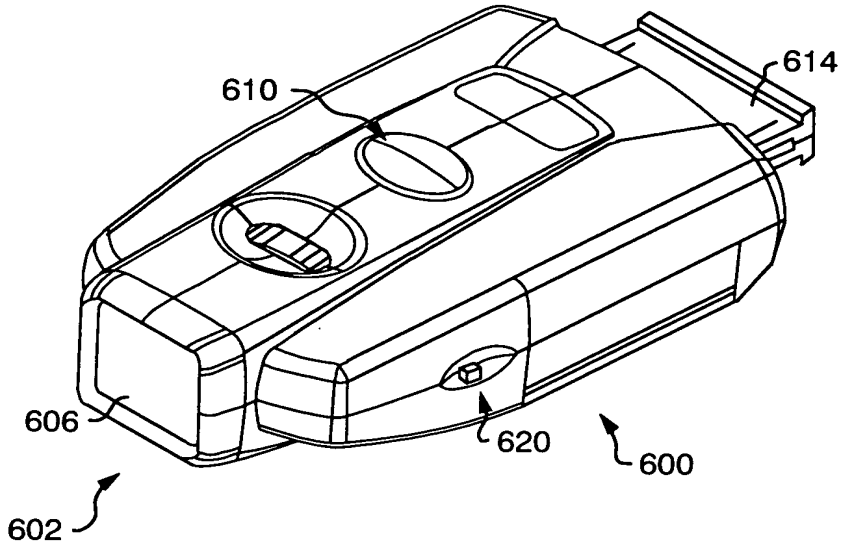


FIG. 34A

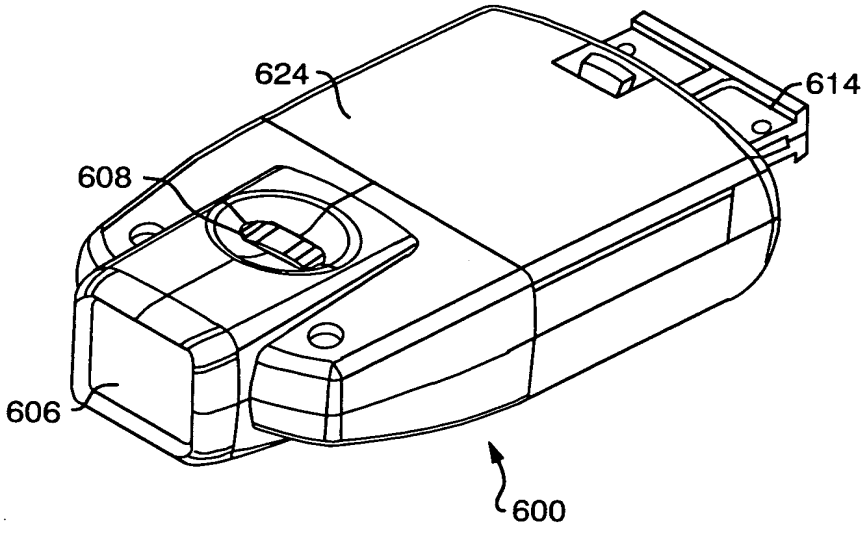


FIG. 34B

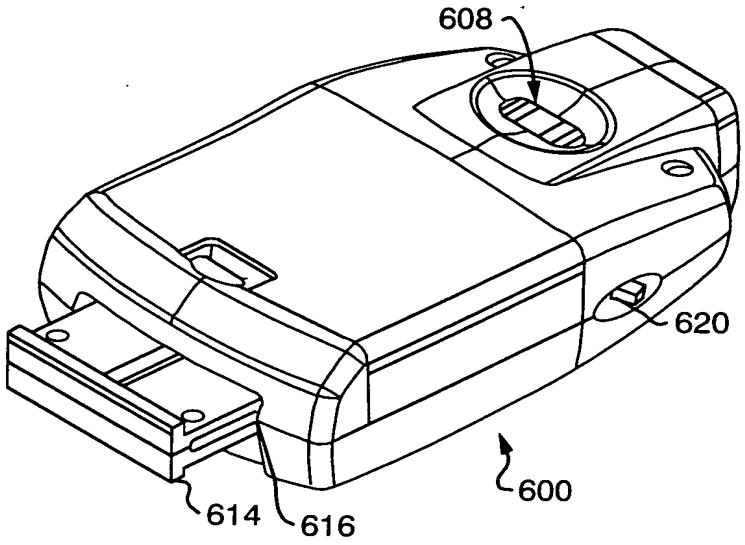


FIG. 34C

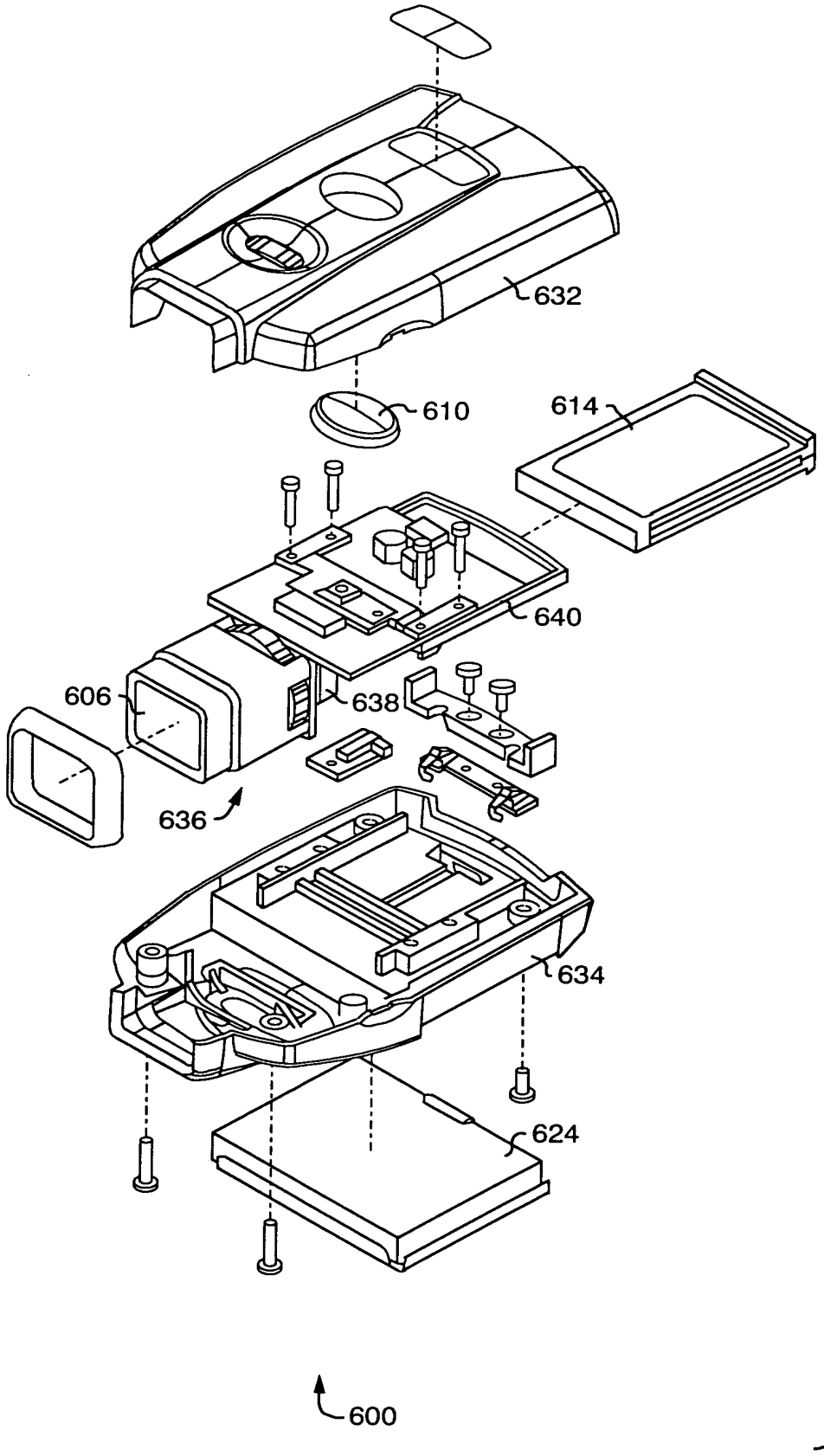


FIG. 34D

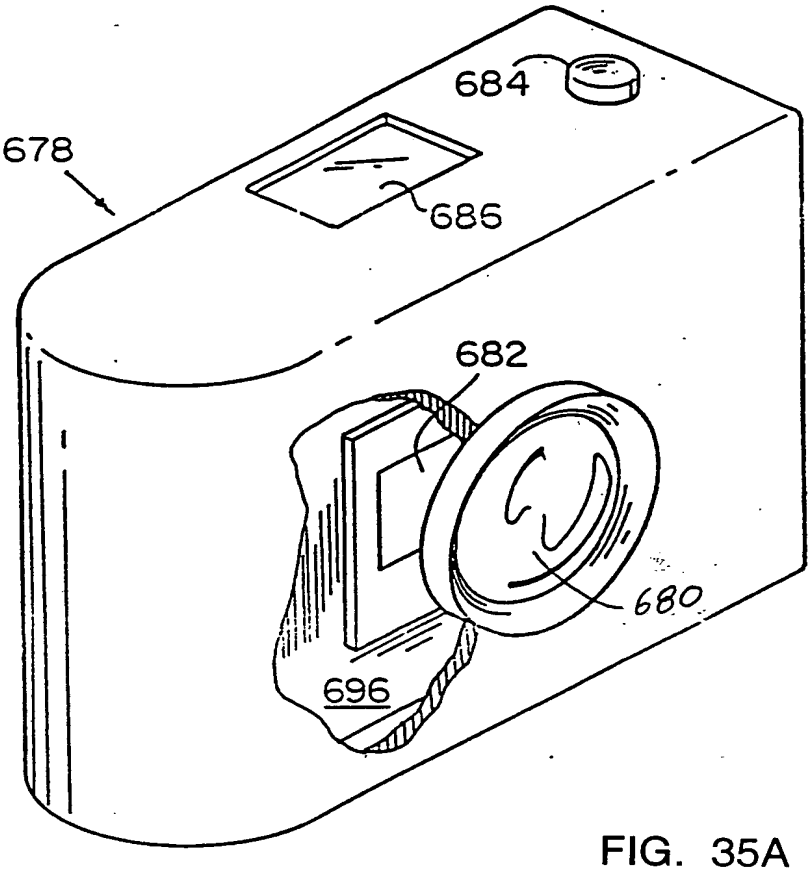


FIG. 35A

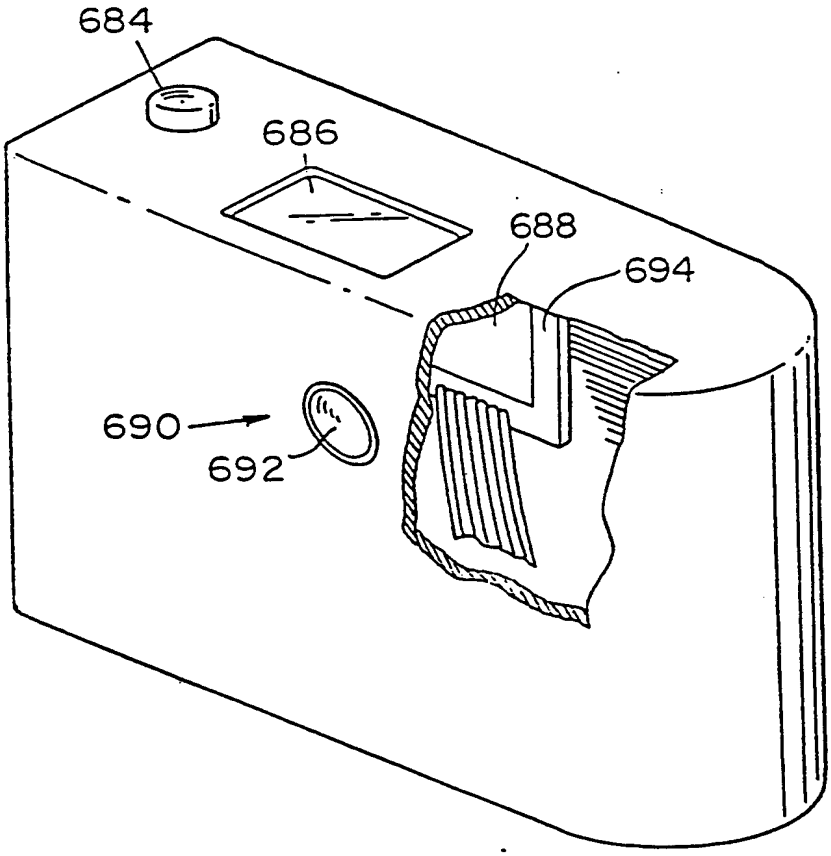


FIG. 35B

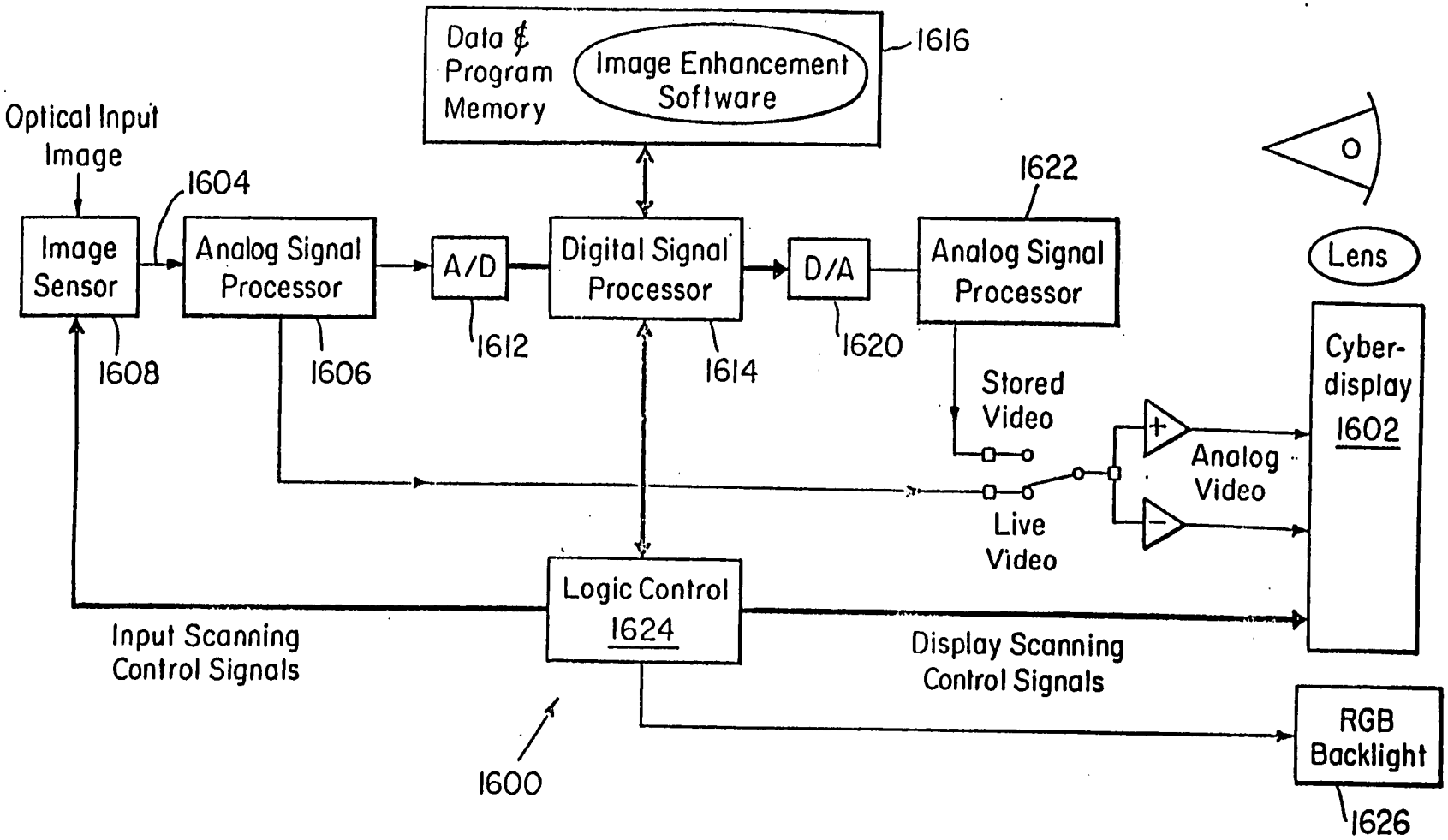

Data & Program Memory
Image Enhancement Software
1616
Optical Input Image
1604
Image Sensor
Analog Signal Processor
A/D
Digital Signal Processor
D/A
Analog Signal Processor
1622
Lens
1608
1606
1612
1614
1620
Stored Video
Cyber-display 1602
Analog Video
Live Video
Logic Control 1624
Input Scanning Control Signals
Display Scanning Control Signals
RGB Backlight
1626
1600

FIG. 35C

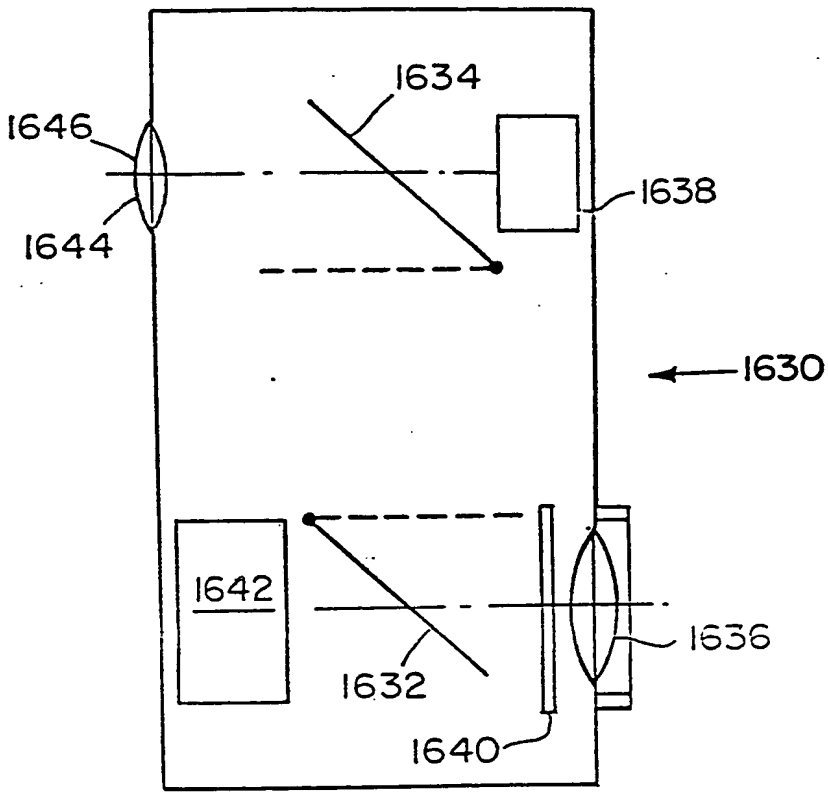


FIG. 35D

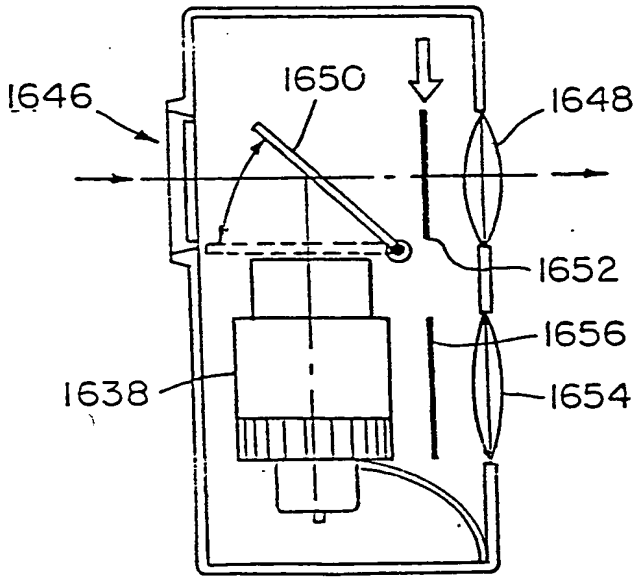


FIG. 35E

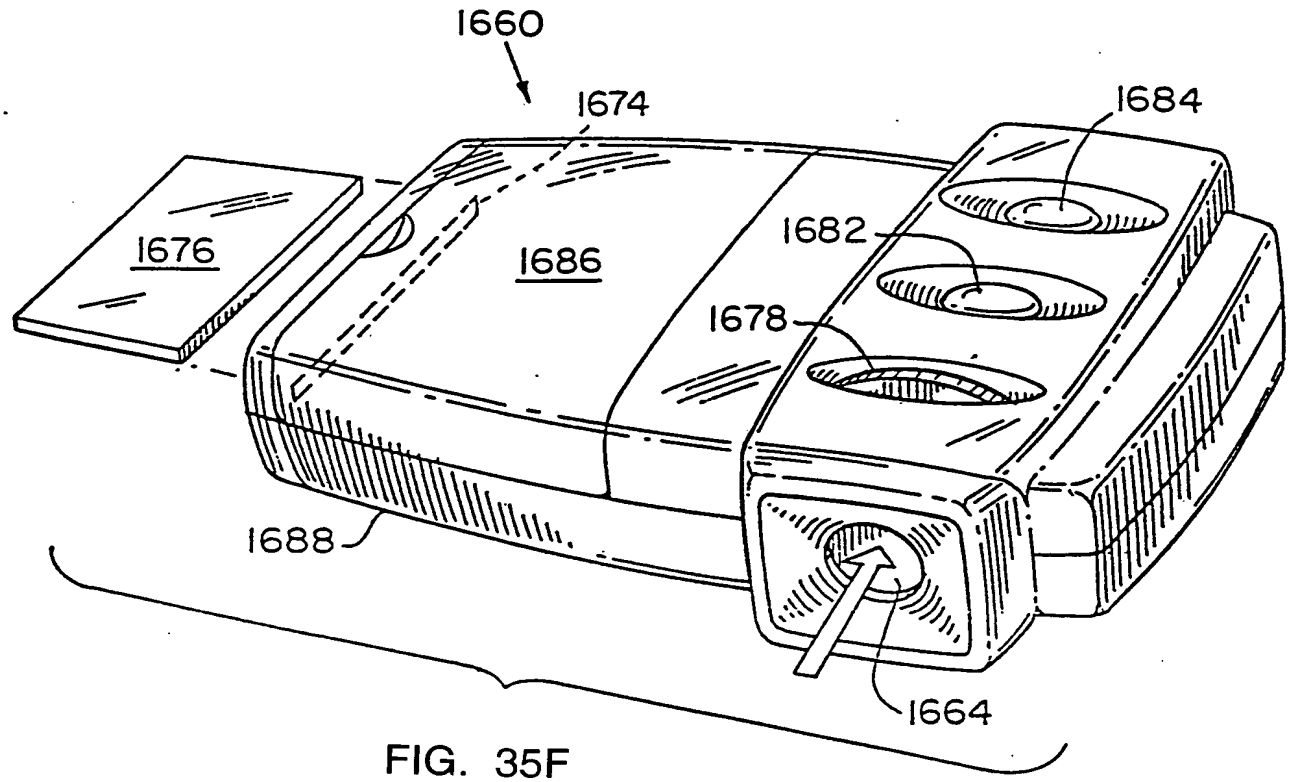


FIG. 35F

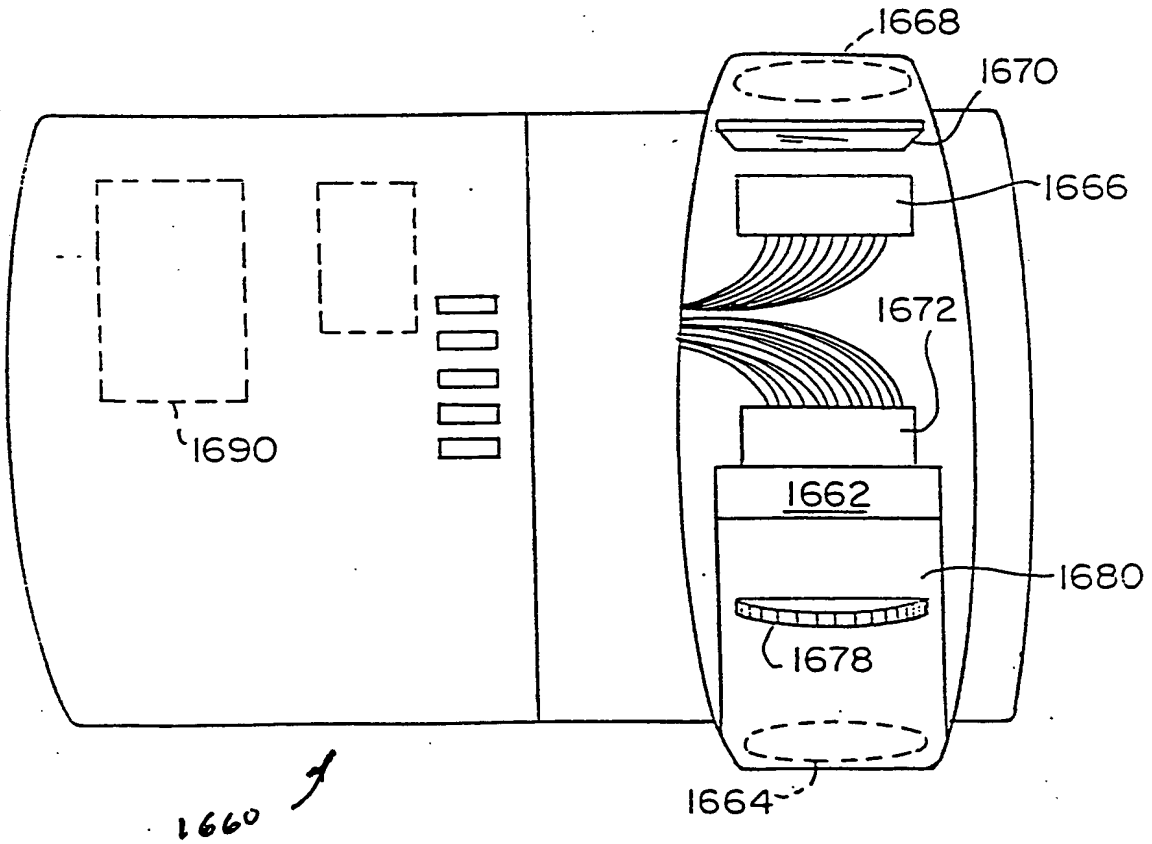


FIG. 35G

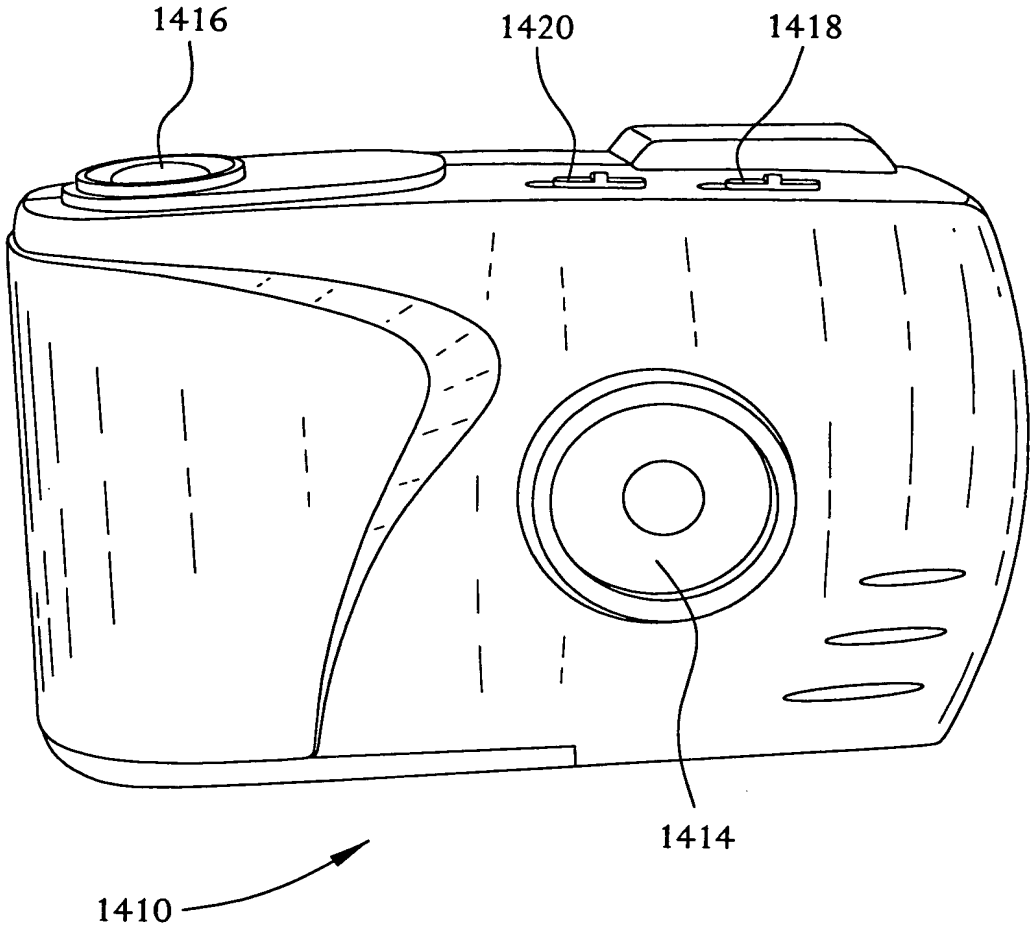


FIG. 35H

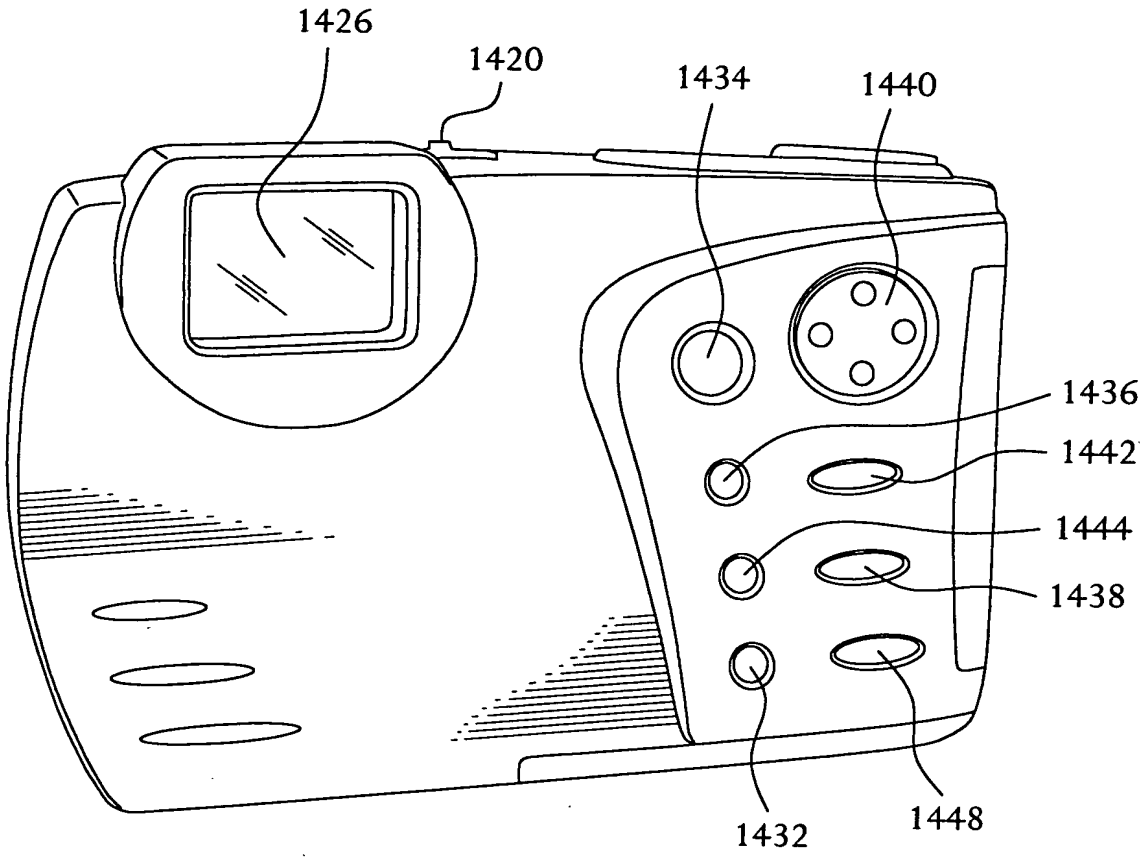


FIG. 35I

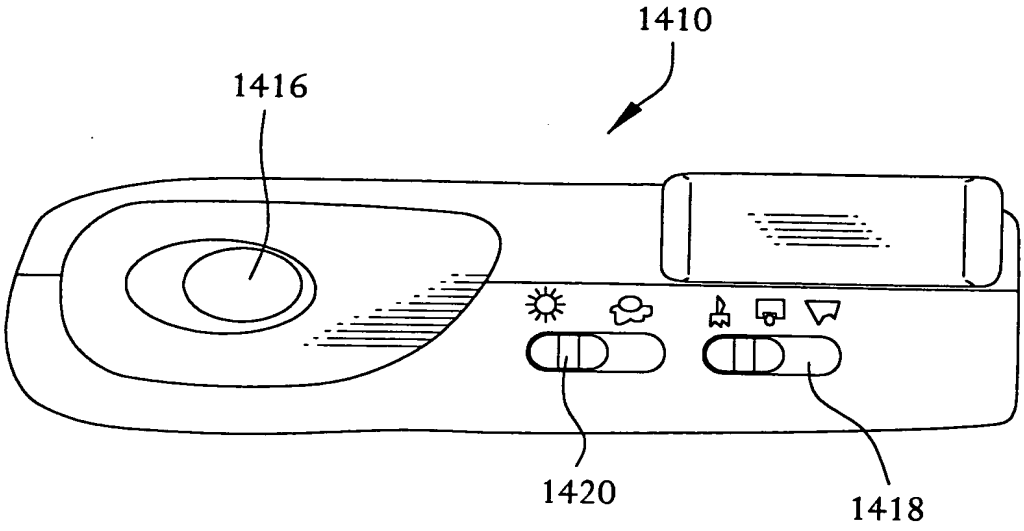


FIG. 35J

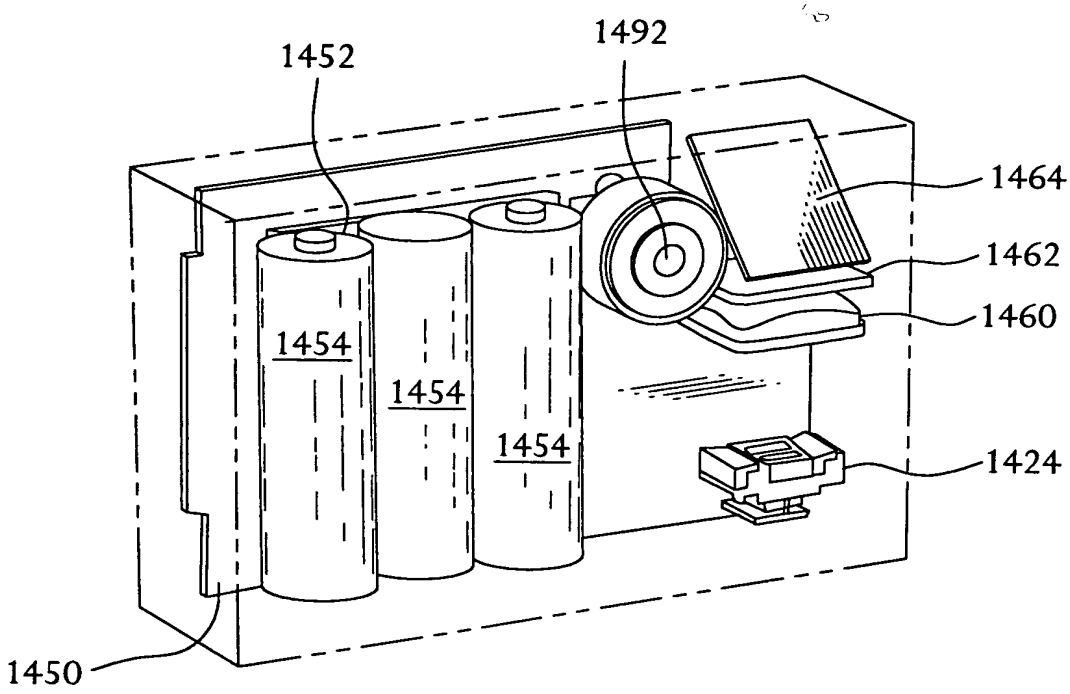


FIG. 35K

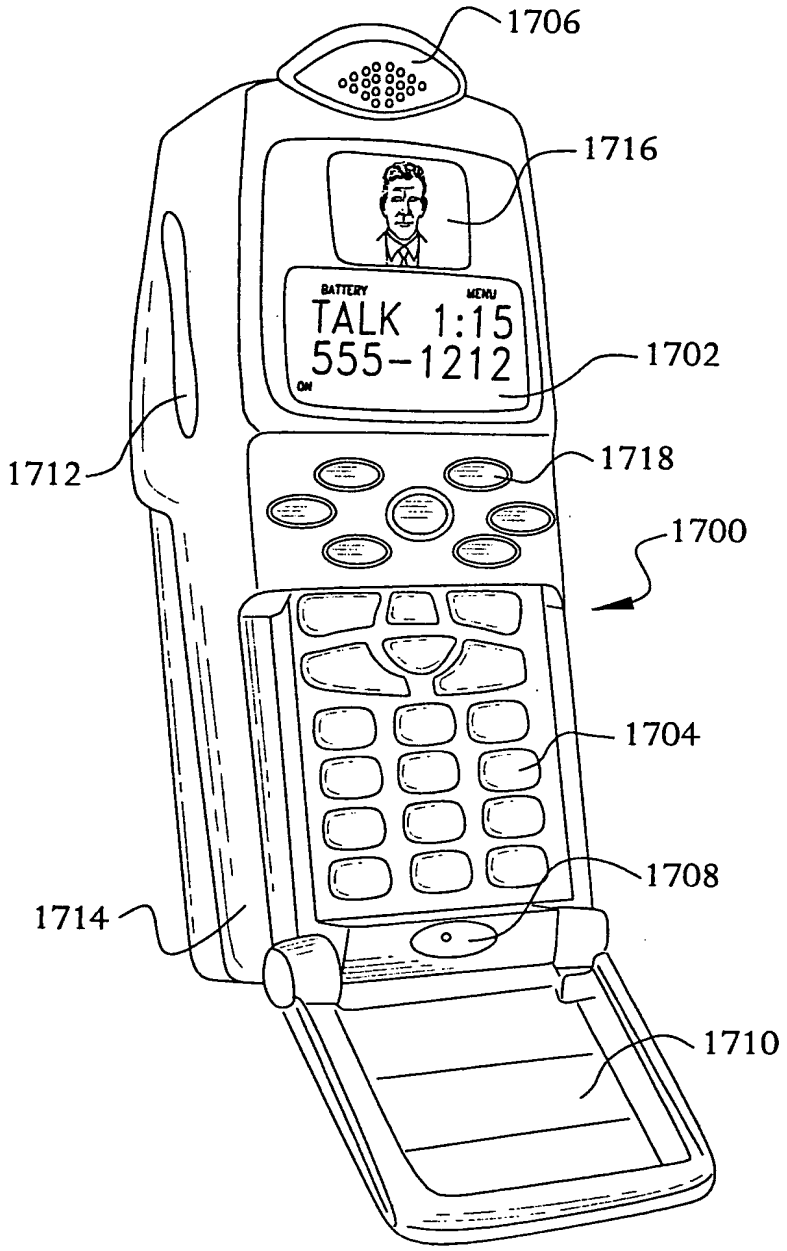

1706
1716
BATTERY
MENU
TALK 1:15
555-1212
ON
1702
1712
1718
1700
1704
1708
1714
1710

FIG. 36A

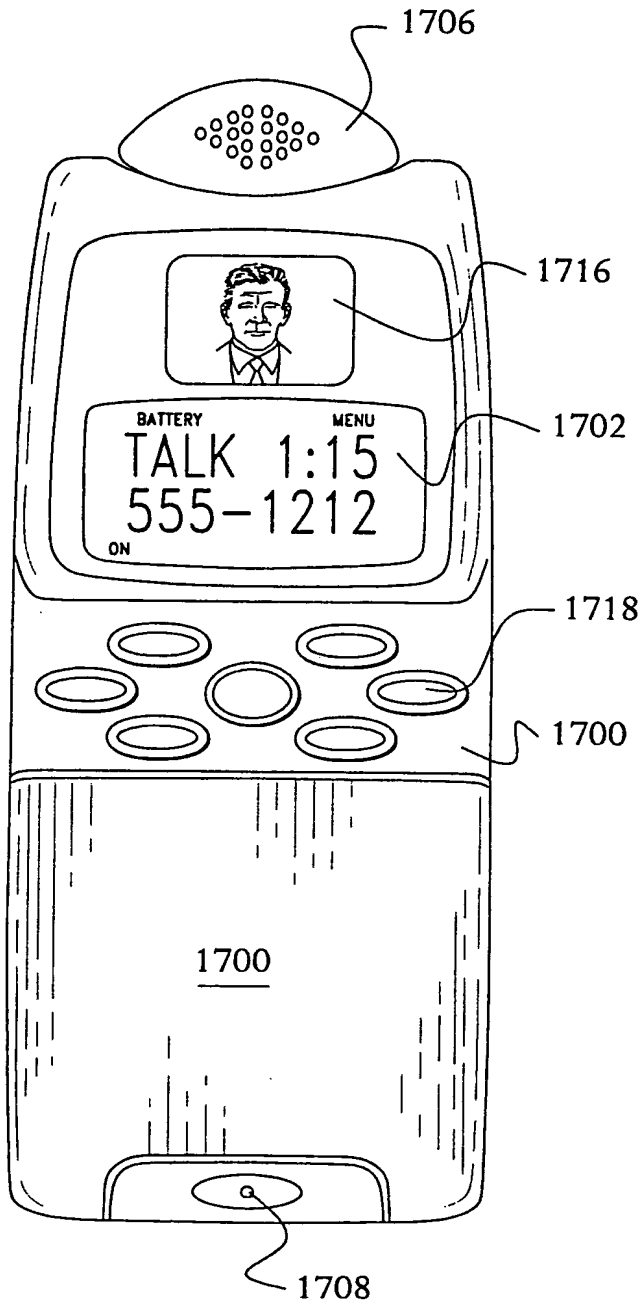

1706
1716
BATTERY
MENU
TALK 1:15
555-1212
ON
1702
1718
1700
1700
1708

FIG. 36B

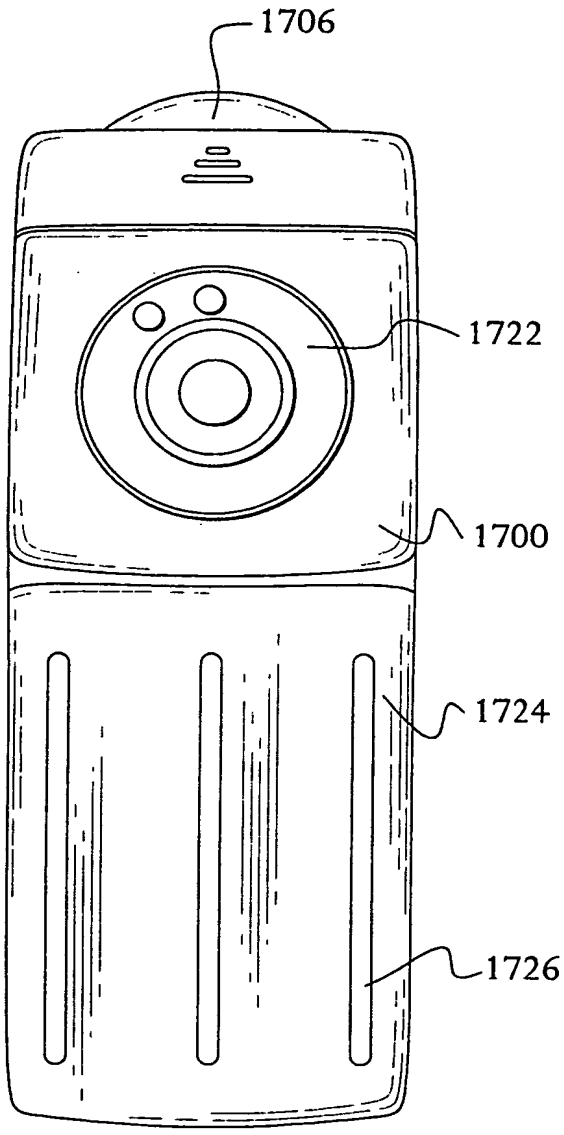


FIG. 36C

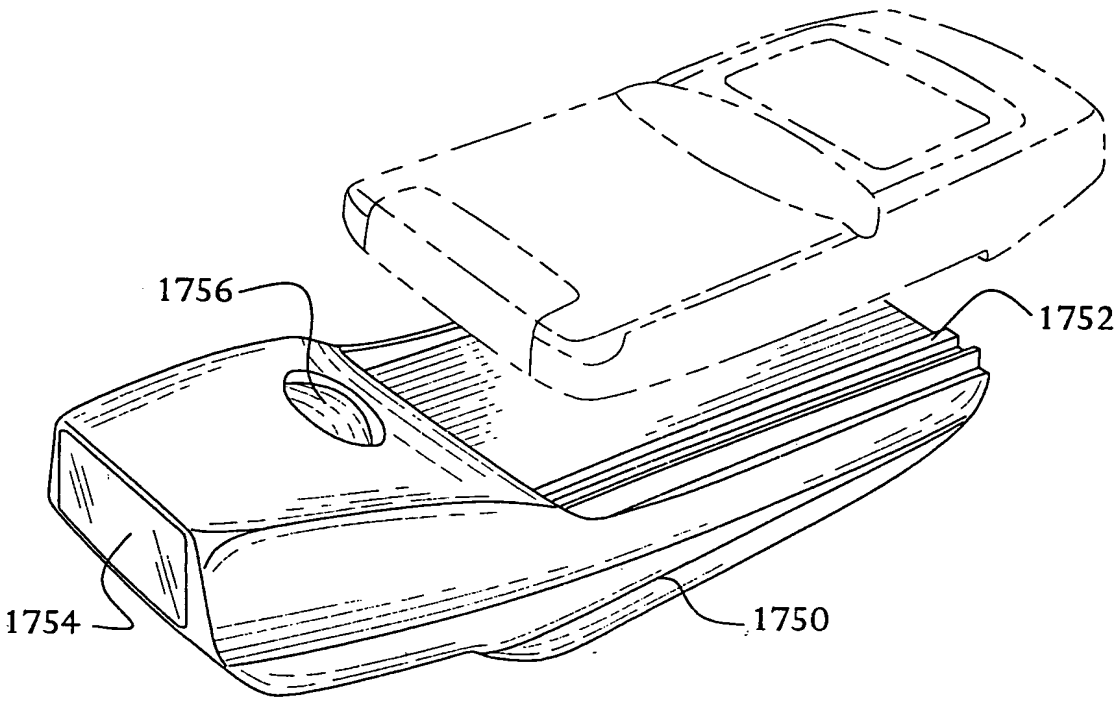


FIG. 37A

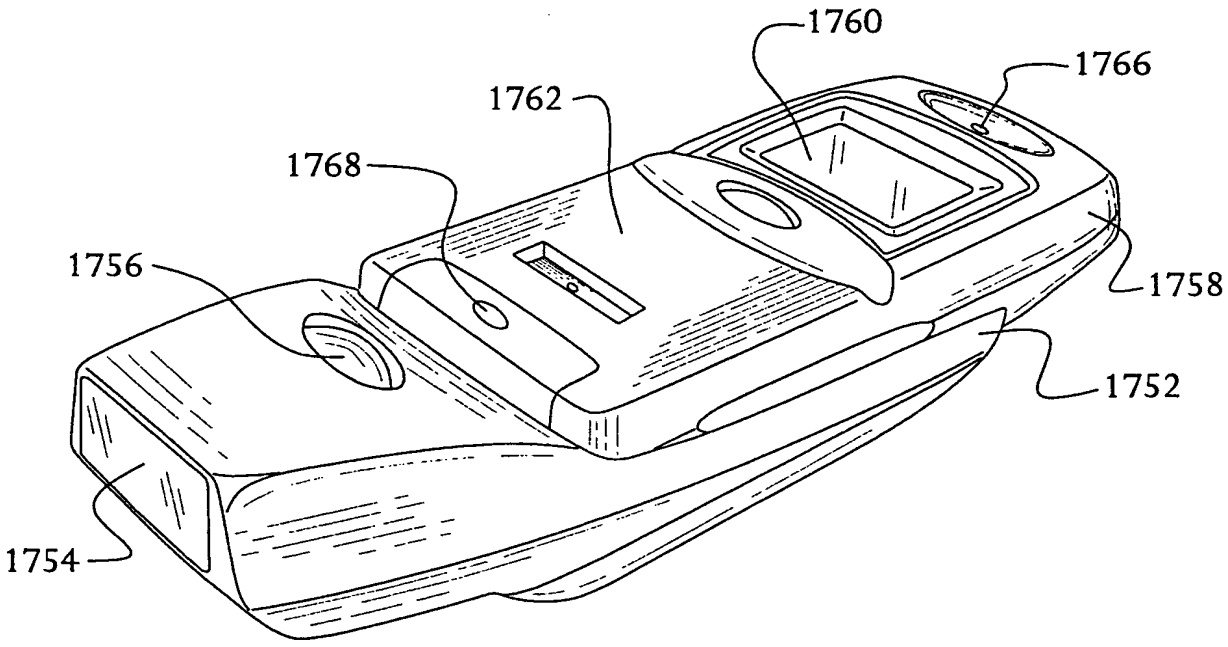


FIG. 37B

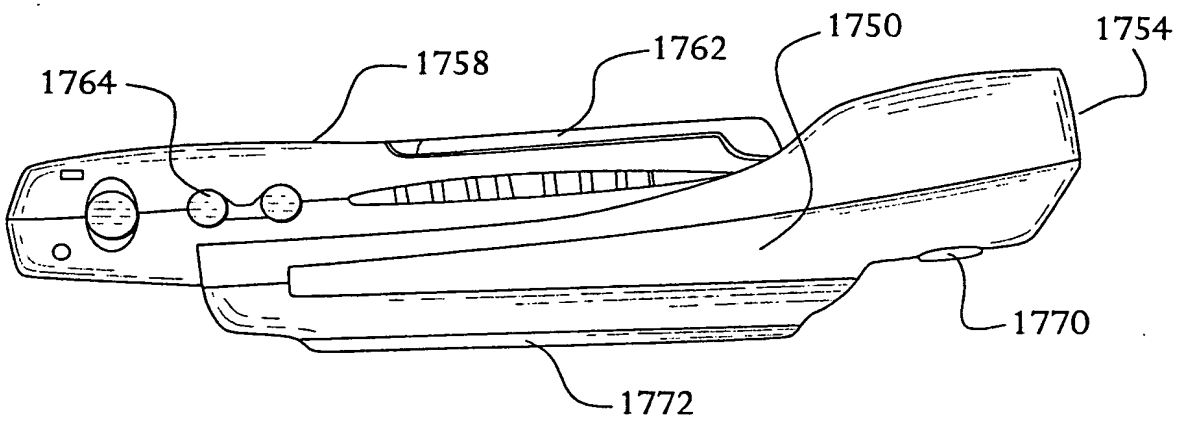


FIG. 37C

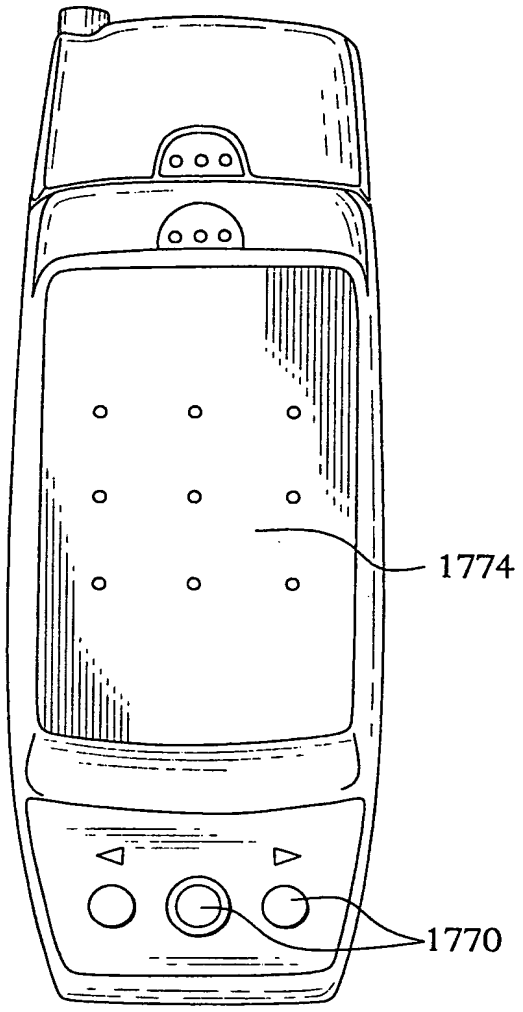


FIG. 37D

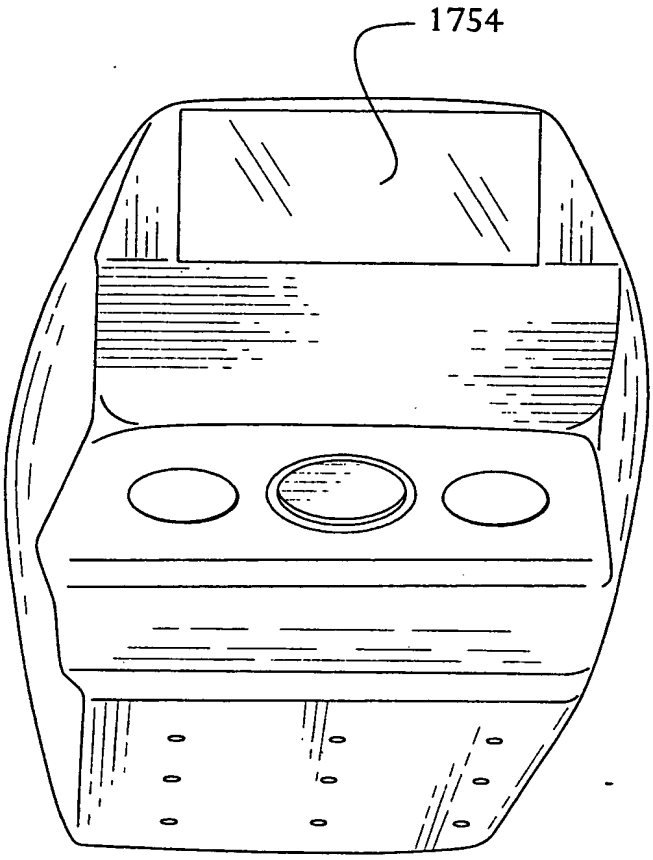


FIG. 37E

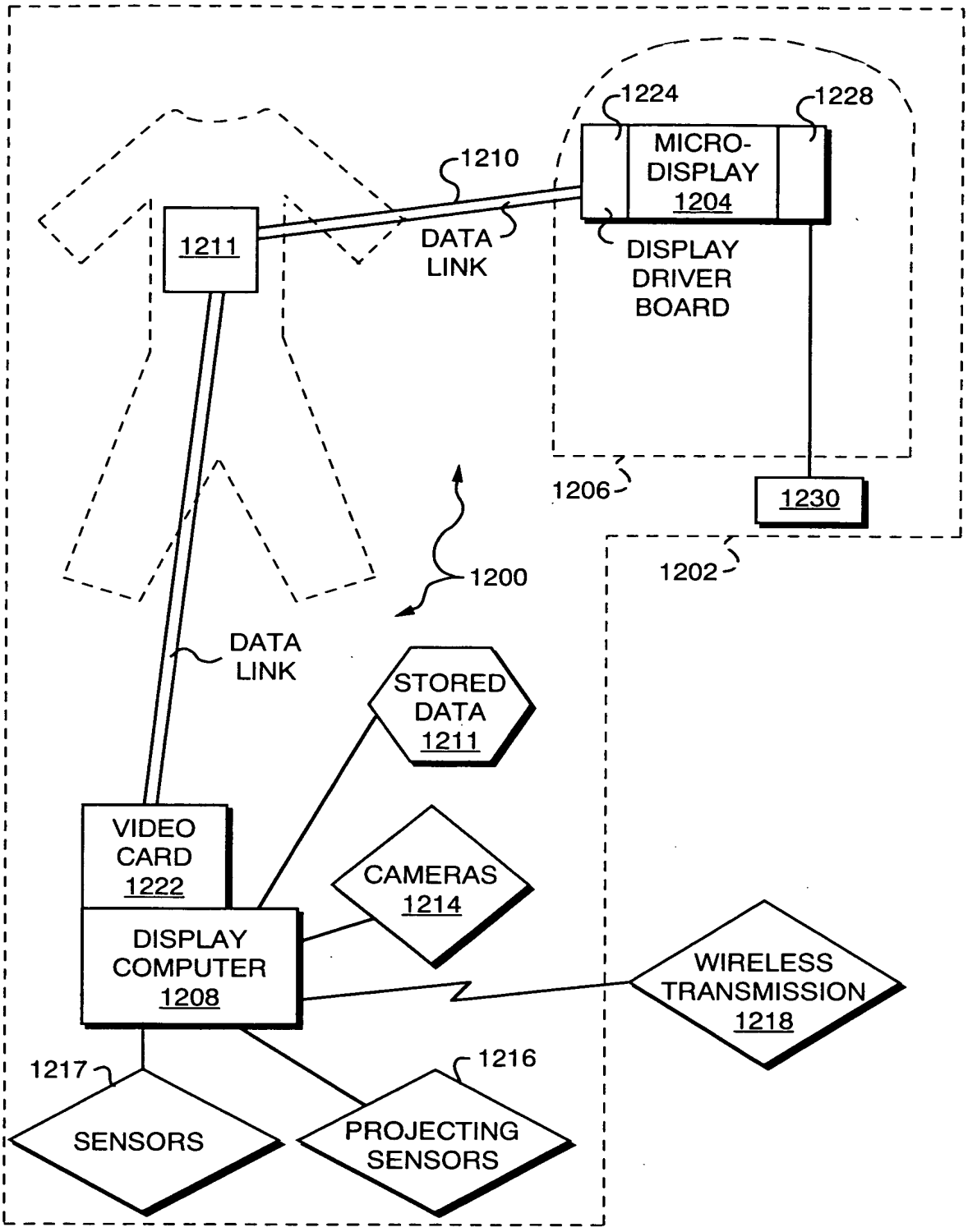

1224
1228
MICRO-
DISPLAY
1204
1210
1211
DATA
LINK
DISPLAY
DRIVER
BOARD
1206
1230
1202
1200
DATA
LINK
STORED
DATA
1211
VIDEO
CARD
1222
CAMERAS
1214
DISPLAY
COMPUTER
1208
WIRELESS
TRANSMISSION
1218
1217
1216
SENSORS
PROJECTING
SENSORS

FIG. 38A

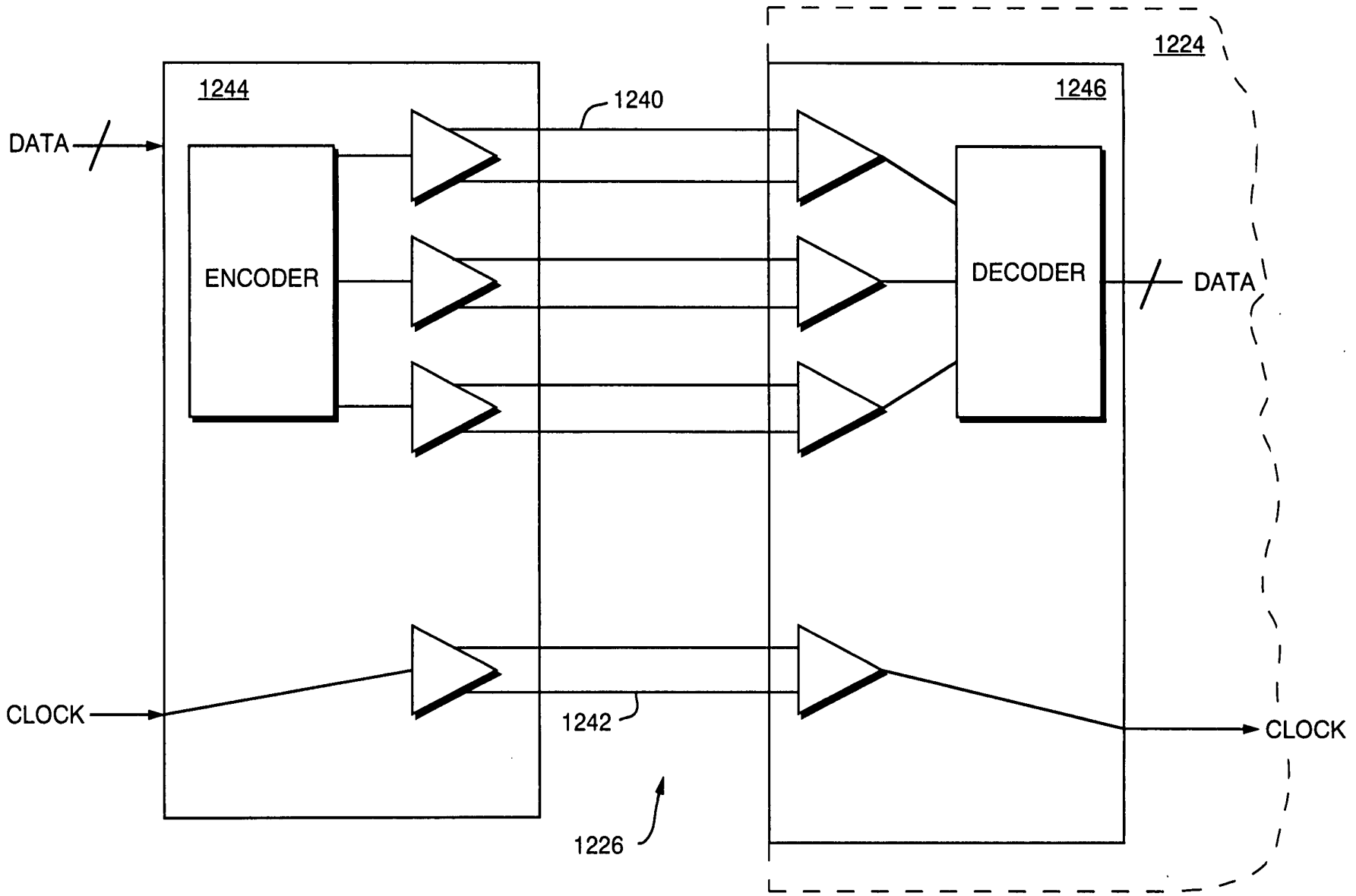


FIG. 38B

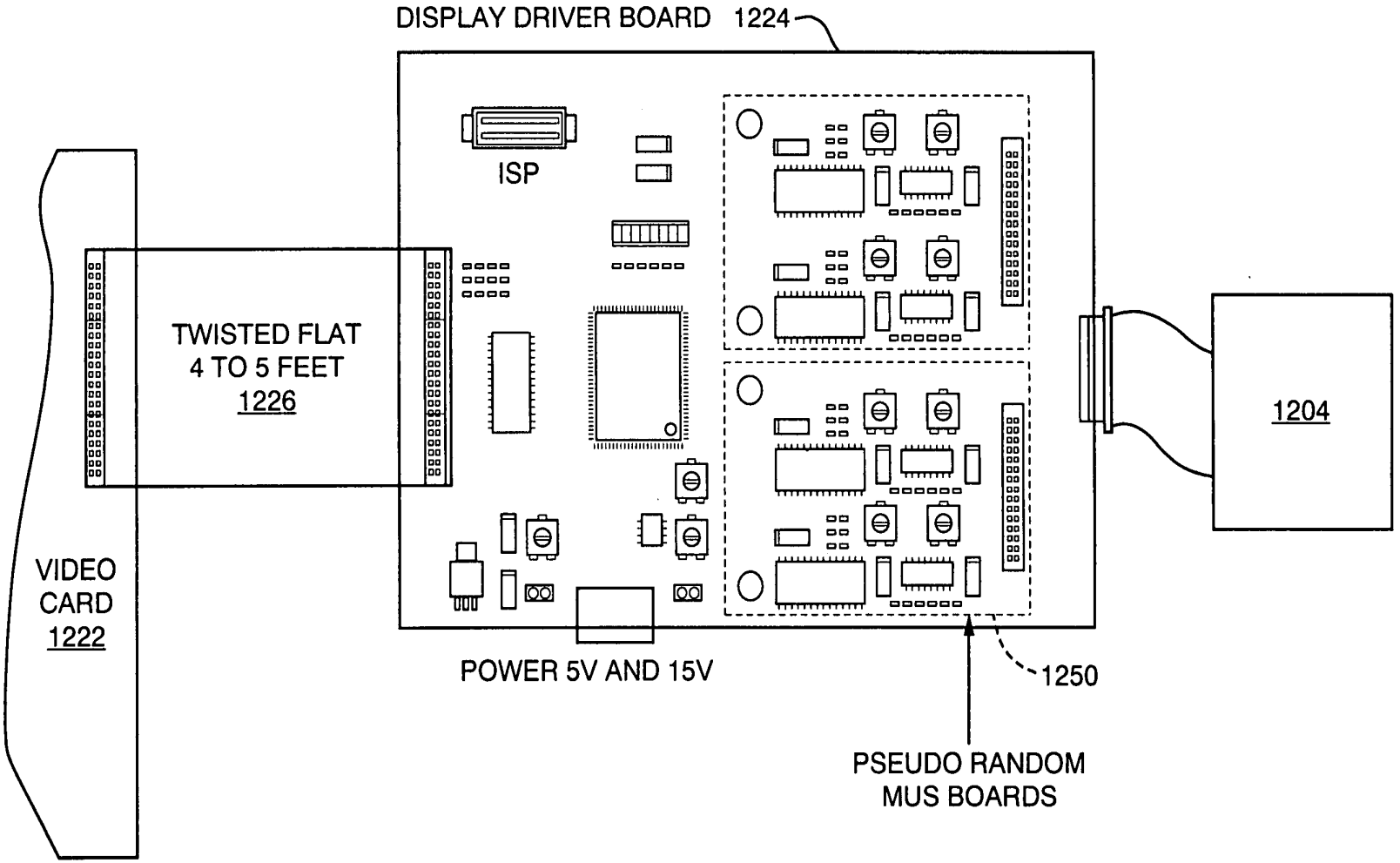


FIG. 38C

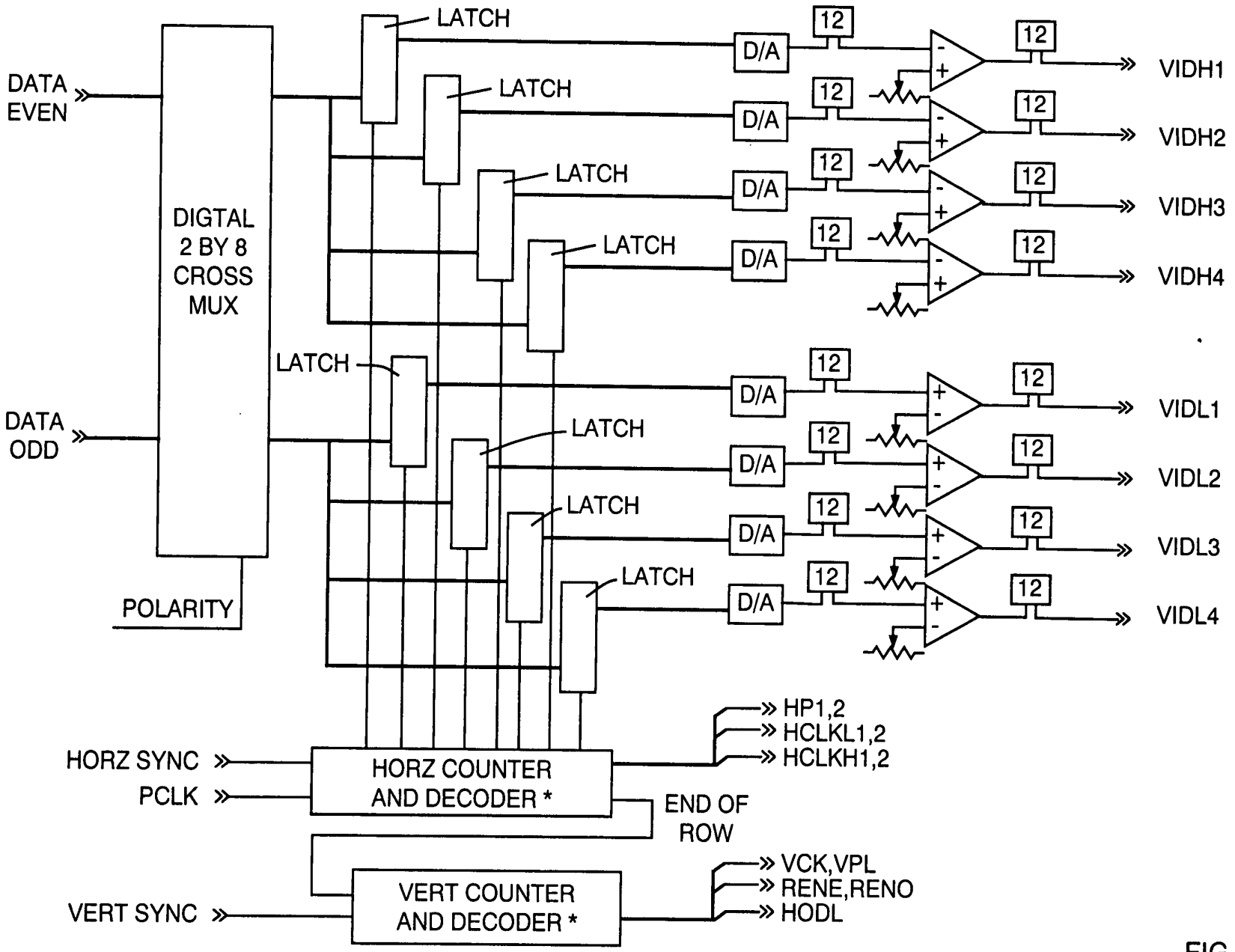


FIG. 38D

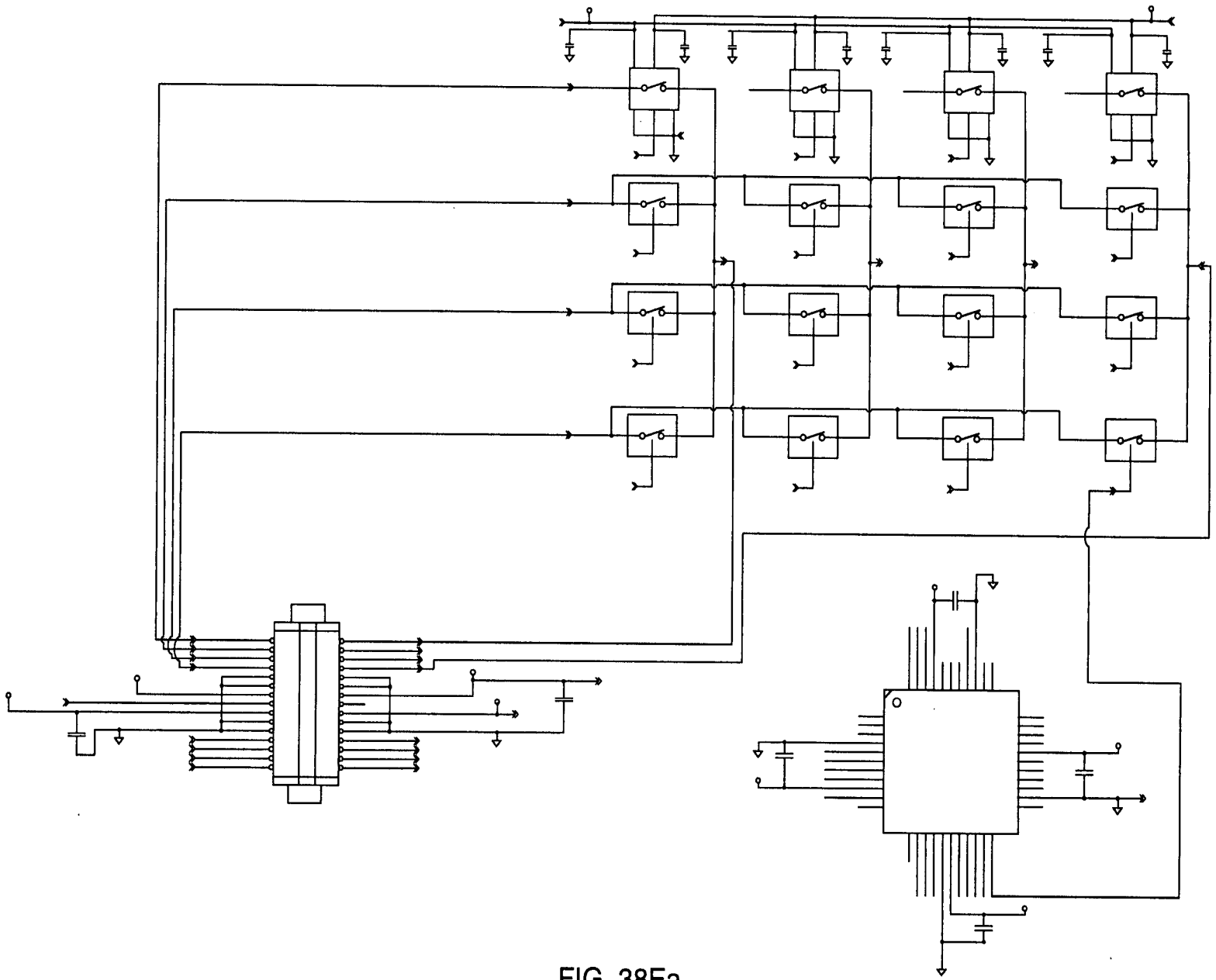


FIG. 38Ea

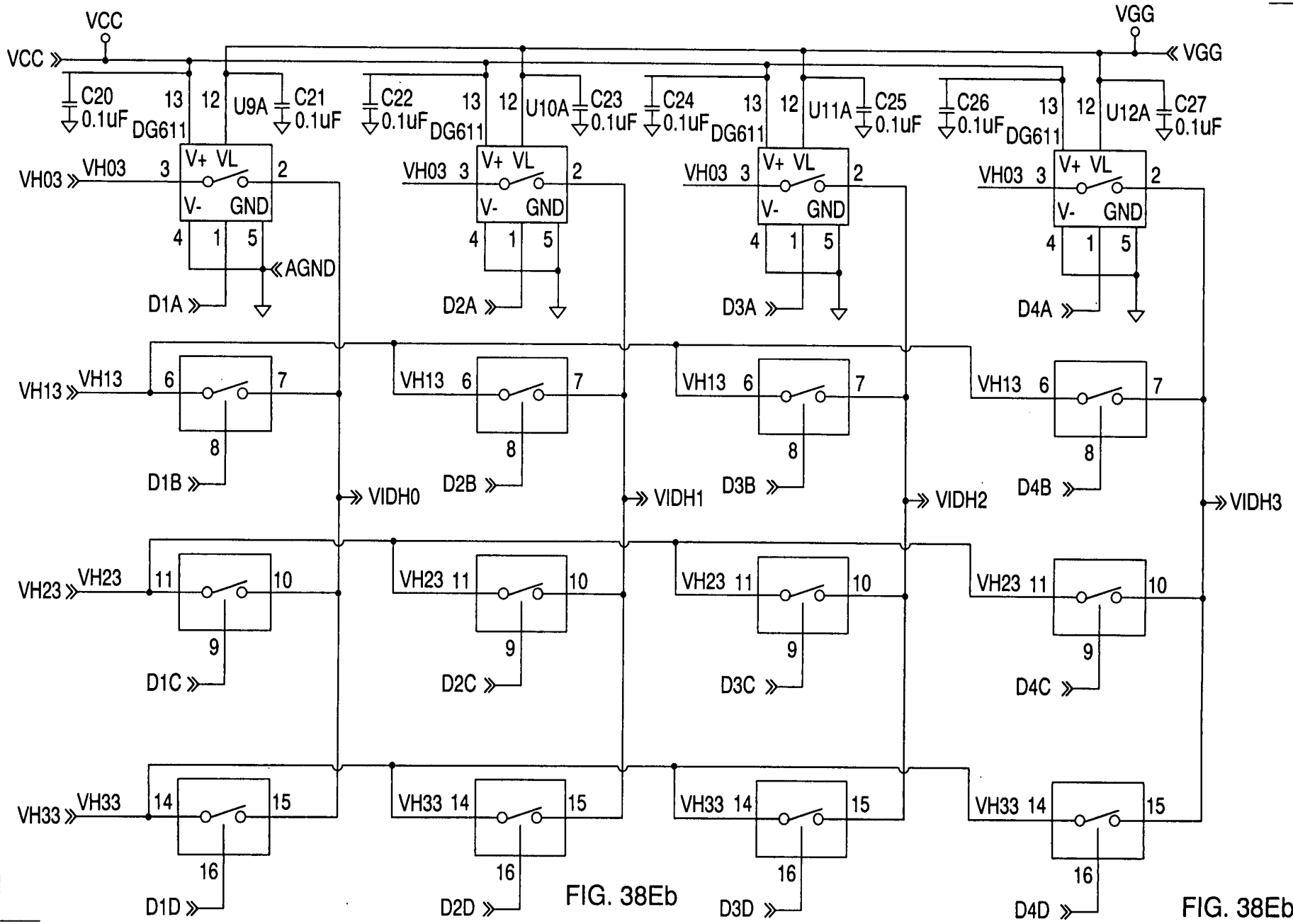


FIG. 38Eb

FIG. 38Eb